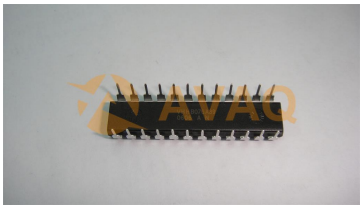
EP610PC-25T

CPLD Classic Family 300 Gates 16 Macro Cells 40MHz 5V 24-Pin PDIP T/R



Images are for reference only

Inquiry

Manufacturer:	Rochester Electronics Incorporated
Package/Case:	DIP
Product Type:	Programmable Logic ICs
Lifecycle:	Aftermarket

General Description

The Altera ClassicTM EP610 device offers a solution to high-speed, lowpower logic integration. Fabricated on advanced CMOS technology, EP610 devices also have a Turbo-only version, which is described in this data sheet.

Classic devices support 100% TTL emulation and can easily integrate multiple PAL- and GAL-type devices with densities ranging from 300 to 900 usable gates. The Classic family provides pin-to-pin logic delays as low as 10 ns and counter frequencies as high as 100 MHz. Classic devices are available in a wide range of packages, including ceramic dual in-line package (CerDIP), plastic dual in-line package (PDIP), plastic J-lead chip carrier (PLCC), ceramic J-lead chip carrier (JLCC), pin-grid array (PGA), and small-outline integrated circuit (SOIC) packages.

EP610 devices have 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global clock pins. Each macrocell can access signals from the global bus, which consists of the true and complement forms of

the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. The CLK1 signal is a dedicated global clock input for the registers in macrocells 9 through 16. The CLK2 signal is a dedicated global clock input for registers in macrocells 1 through 8.

EPROM-based Classic devices can reduce active power consumption without sacrificing performance. This reduced power consumption makes the Classic family well suited for a wide range of low-power applications.

Classic devices are 100% generically tested devices in windowed packages and can be erased with ultra-violet (UV) light, allowing design changes to be implemented quickly. Classic devices use sum-of-products logic and a programmable register. The sum-of-products logic provides a programmable-AND/fixed-OR structure that can implement logic with up to eight product terms. The programmable register can be individually programmed for D, T, SR, or JK flipflop operation or can be bypassed for combinatorial operation. In addition, macrocell registers can be individually clocked either by a global clock or by any input or feedback path to the AND array. Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to implement a variety of logic functions simultaneously.

Classic devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstationbased EDA tools. The MAX+PLUS II software runs on Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations. These devices also contain on-board logic test circuitry to allow verification of function and AC specifications during standard production flow.

Key Features

High-performance, 16-macrocell Classic EPLD

t

PD

as fast as 10 ns

Programmable I/O architecture with up to 20 inputs or 16 outputs and 2 clock pins

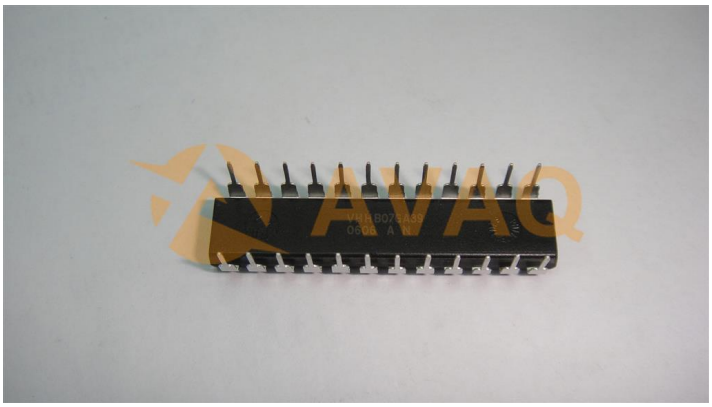
EP610 and EP610I devices are pin-, function-, and programming file-compatible

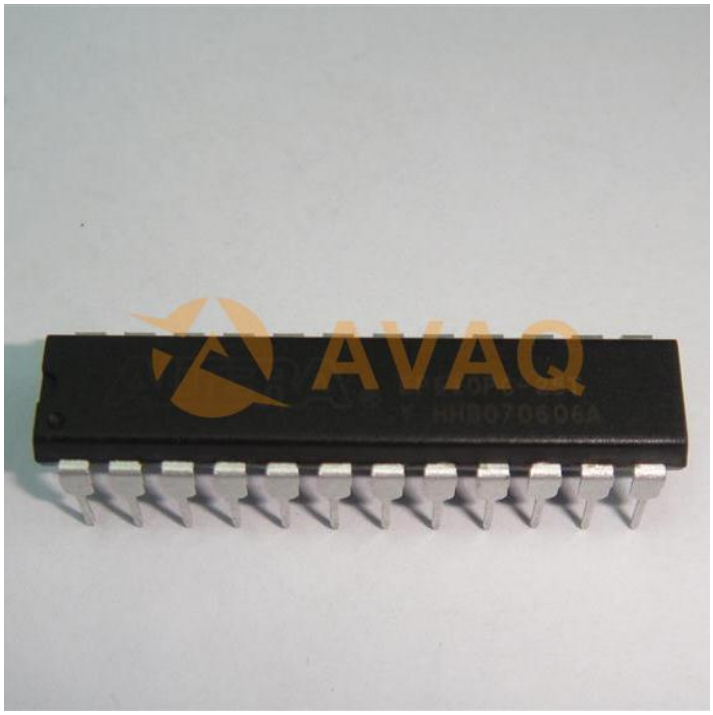
Programmable clock option for independent clocking of all registers

Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation

Available in the following packages (see

Figure 7





Recommended For You

EP610PC-30

Rochester Electronics Incorporated

DIP

EP610PI-30

Rochester Electronics Incorporated

DIP24

EP1810LI-45

Rochester Electronics Incorporated

PLCC68

EP600IPC-45

Rochester Electronics Incorporated

DIP

EP610LC-15

Rochester Electronics Incorporated

PLCC28

EP610PC-35

Rochester Electronics Incorporated

DIP

EP900IPC-50

Rochester Electronics Incorporated

DIP40

EP610LC-35

Rochester Electronics Incorporated

PLCC

EP910LI-35

Rochester Electronics Incorporated

PLCC

EP610LI-30

Rochester Electronics Incorporated

PLCC

EP610DC-30

Rochester Electronics Incorporated

CWDIP24

EP600IDC-45

Rochester Electronics Incorporated

DIP

EP610DC-25

Rochester Electronics Incorporated

DIP

EP910LC-40

Rochester Electronics Incorporated

PLCC44

EP1800ILC-70

Rochester Electronics Incorporated

PLCC68