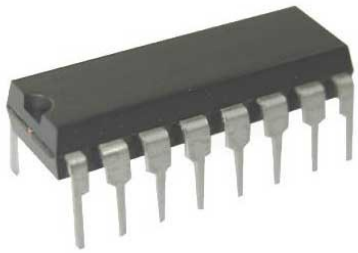
CD40192BE

Counter Single 4-Bit Async Decade UP/Down 16-Pin PDIP Tube

Manufacturer:	Texas Instruments, Inc
Package/Case:	DIP16
Product Type:	Logic ICs
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active



Images are for reference only

Inquiry

General Description

CD40192b Presettable BCD Up/Down Counter and the CD40193B Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a PRESET\ ENABLE\ control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as CARRY\ and BORROW\ outputs for multiple-stage counting schemes are provided. The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the PRESET\ ENABLE\ control is low. The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down on count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

The CARRY\ and BORROW\ signals are high with the counter is counting up or down. The CARRY\ signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The BORROW\ signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished with out the need for additional external circuitry by tying the BORROW\ and CARRY\ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

The CD40192B and CD40193B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Key Features

Individual clock lines for counting up or counting down

Synchronous high-speed carry and borrow propagation delays for cascading

Asynchronous reset and preset capability

Medium-speed operation–fCL = 8MHz (typ.) @ 10 V

5-V, 10-V, and 15-V parametric ratings

Standardized, symmetrical output characteristics

100% tested for quiescent current at 20 V

Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C

Noise margin (full package-temperature range) = 1 V at VDD = 5 V 2 V at VDD = 10 V2.5 V at VDD = 15 V

Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:
Up/down difference counting

Multistage ripple counting

Synchronous frequency dividers

A/D and D/A conversion

Programmable binary or BCD counting

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Recommended For You

CD4017BE	**CD40193BE**	**CD4024BM**
Texas Instruments, Inc	Texas Instruments, Inc	Texas Instruments, Inc
DIP16	DIP	SOP14

CD74AC161M

Texas Instruments, Inc

SOP16

CD4060BM

Texas Instruments, Inc

SOP

CD4520BE

Texas Instruments, Inc

DIP16

CD4040BE

Texas Instruments, Inc

DIP16

CD4026BE

Texas Instruments, Inc

DIP

CD4516BE

Texas Instruments, Inc

DIP16

CD4060BE

Texas Instruments, Inc

DIP16

CD4020BE

Texas Instruments, Inc

DIP16

CD40110BE

Texas Instruments, Inc

DIP

CD74HCT193E

Texas Instruments, Inc

DIP

CD4510BNSR

Texas Instruments, Inc

SOP16

CD4022BE

Texas Instruments, Inc

DIP