
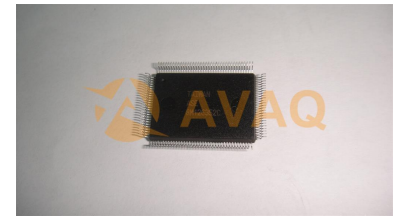


## Ethernet CTLR Single Chip 10Mbps/100Mbps 3.3V 128-Pin QFP Tray

<b>Manufacturer:</b>	<a href="#">Microchip Technology, Inc</a>
<b>Package/Case:</b>	QFP
<b>Product Type:</b>	Communication & Networking ICs
<b>RoHS:</b>	RoHS Compliant/Lead free 
<b>Lifecycle:</b>	Active



Images are for reference only

[Inquiry](#)

### General Description

The Microchip LAN91C111 is designed to facilitate the implementation of a third generation of Fast Ethernet connectivity solutions for embedded applications. For this third generation of products, flexibility and integration dominate the design requirements. The LAN91C111 is a mixed signal Analog/Digital device that implements the MAC and PHY portion of the CSMA/CD protocol at 10 and 100 Mbps. The design will also minimize data throughput constraints utilizing a 32-bit, 16-bit or 8-bit bus Host interface in embedded applications.

The total internal memory FIFO buffer size is 8 Kbytes, which is the total chip storage for transmit and receive operations.

The Microchip LAN91C111 is software compatible with the LAN9000 family of products.

\*The LANCheck online design review service is subject to Microchip's Program Terms and Conditions and requires a myMicrochip account.

For product comparison, please consider:LAN9218

### Key Features

Features

Single Chip Ethernet Controller

Dual Speed - 10/100 Mbps

Fully Supports Full Duplex Switched Ethernet

Supports Burst Data Transfer

8 Kbytes Internal Memory for Receive and Transmit FIFO Buffers

Enhanced Power Management Features

Optional Configuration via Serial EEPROM Interface

Supports 8, 16 and 32 Bit CPU Accesses

Internal 32 Bit Wide Data Path (into Packet Buffer Memory)

Built-in Transparent Arbitration for Slave Sequential Access Architecture

Flat MMU Architecture with Symmetric Transmit and Receive Structures and Queues

3.3V Operation with 5V Tolerant I/O Buffers

Single 25 MHz Reference Clock for Both PHY and MAC

External 25 MHz Output Pin for an External PHY Supporting PHY's Physical Media

Low Power CMOS Design

Supports Multiple Embedded Processor Host Interfaces

ARM

SH

Power PC

Coldfire

680X0, 683XX

MIPS R3000

3.3V MII (Media Independent Interface) MAC-PHY Interface Running at Nibble Rate

MIIM Management Serial Interface

128 Pin QFP RoHS compliant package

128 Pin TQFP 1.0 mm height RoHS compliant package

Commercial Temperature Range from 0°C to 70°C (LAN91C111)

Industrial Temperature Range from -40°C to 85°C (LAN91C111i)

Network Interface

Fully Integrated IEEE 802.3/802.3u - 100BASE-TX/10BASE-T Physical Layer

Auto Negotiation: 10/100, Full/Half Duplex

On Chip Wave Shaping - No External Filters Required

Adaptive Equalizer

Baseline Wander Correction

LED Outputs (User Selectable - Up to Two LED Functions at One Time)

Link

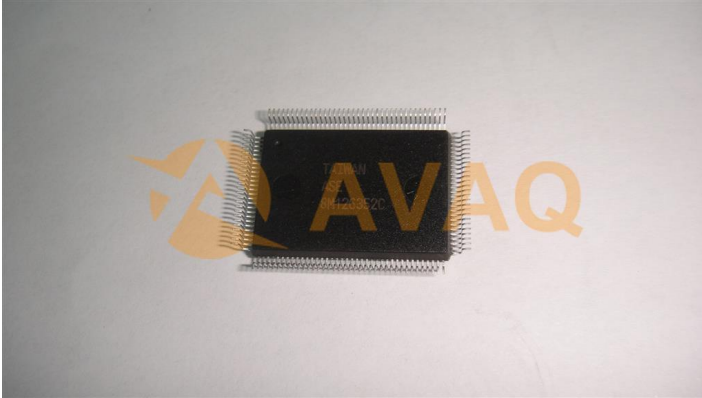
Activity

Full Duplex

10/100

Transmit

Receive



## Recommended For You

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### LAN91C111-NE

Microchip Technology, Inc

QFP

### LAN91C93I-MU

Microchip Technology, Inc

QFP

### LAN9420I-NU

Microchip Technology, Inc

TQFP128

### LAN91C96-MU

Microchip Technology, Inc

TQFP100

### LAN91C111i-NC

Microchip Technology, Inc

QFP

### LAN91C96-MS

Microchip Technology, Inc

QFP

### LAN91C111I-NU

Microchip Technology, Inc

TQFP128

### LAN91C111-NC

Microchip Technology, Inc

QFP

### LAN9252I/ML

Microchip Technology, Inc

QFN-64

### LAN9215-MT

Microchip Technology, Inc

QFP100

### LAN91C111I-NS

Microchip Technology, Inc

QFP128

### LAN91C111-NU

Microchip Technology, Inc

QFP

### LAN9118-MT

Microchip Technology, Inc

TQFP100

### LAN9252I/PT

Microchip Technology, Inc

TQFP64

### LAN9221I-ABZJ

Microchip Technology, Inc

QFN56