Application Report
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Powering the Freescale™ i.MX25 Using the TPS65051

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ABSTRACT

This application report details the power requirements of the Freescale™ i.MX25 processor and how to power it using the TPS65051, a highly-integrated power management unit (PMU) device from Texas Instruments. With its 3.3-V to 6.0-V input voltage range, output current up to 600 mA, and excellent efficiency (up to 95%), the TPS65051 PMU is an excellent choice to meet the requirements of the i.MX25.

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1 Introduction

The reference design discussed in this report applies to the entire Freescale™ i.MX25 processor family. It provides all required analog and logic supply rails and the sequencing necessary to power up an i.MX25 processor.

2 i.MX25 Requirements

Table 1 lists the voltage requirements of the i.MX25 processor.

Table 1. i.MX25 Voltage Requirements[(1)]

Parameter	Symbol	Min	Typ	Max	Units
Core supply voltage (at 266 MHz)	QV_{DD}	1.15	1.34	1.52	V
Core supply voltage (at 400 MHz)	QV_{DD}	1.38	1.45	1.52	V
Coin battery	V_{DD_BAT}	1.15	—	1.55	V
I/O supply voltage GPIO1 (NFC, CSI, SDIO)	NV_{DD_GPIO1}	1.75	—	3.6	V
I/O supply voltage GPIO2 (CRM, LCDC, JTAG, MISC)	NV_{DD_GPIO2}	3.0	3.3	3.6	V
I/O supply voltage DDR (Mobile DDR mode) (EMI1, EMI2)	NV_{DD_MDDR}	1.75	—	1.95	V
I/O supply voltage DDR (DDR2 mode) (EMI1, EMI2)	NV_{DD_DDR2}	1.75	—	1.9	V
I/O supply voltage DDR (SDRAM mode) (EMI1, EMI2)	NV_{DD_SDRAM}	1.75	—	3.6	V
USBPHY1 supply (HS) (USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD. USBPHY1_VDDA)	$V_{DD\_USBPHY1}$	3.17	3.3	3.43	V
USBPHY2 supply (FS) (USBPHY2_VDD)	$V_{DD\_USBPHY2}$	3.0	3.3	3.6	V
OSC24M supply (OSC24M_VDD)	V_{DD_OSC24M}	3.0	3.3	3.6	V
PLL supply (MPLL_VDD, UPLL_VDD)	V_{DD_PLL}	1.4	—	1.65	V
Supply of touch screen ADC (NVCC_ADC)	V_{DD_TSC}	3.0	3.3	3.6	V
External reference of touch screen ADC	V_{REF}	2.5	V_{DD_tsc}	V_{DD_tsc}	V
Fusebox program supply voltage (FUSE_VDD)	$FUSEV_{DD}$	—	3.6	—	V

(1) See Reference 1 for complete information.

2.1 Power-Up/-Down Sequencing

The i.MX25 processor consists of four major sections for the power-supply voltage: digital logic domains (V_{DDn}); I/O power supplies (NV_{DDx}); analog power supplies; and the fuse voltage supply ($FUSEV_{DD}$). These voltage groups can be integrated in several ways, depending on the operating mode and the requirements of the i.MX processor, as well as the specific application.

2.1.1 Power-Up Sequencing

The recommended power-up sequence for the processor follows this order:

Step 1. Assert Power-On-Reset (POR) (POR = low)

Step 2. Turn on the core supply voltages and I/O power supplies (NV_{CCx})

Step 3. Turn on all analog power supplies (V_{DDx}) and $FUSEV_{DD}$

Step 4. Release POR (POR = high)

Figure 1 illustrates the recommended power-up sequence.

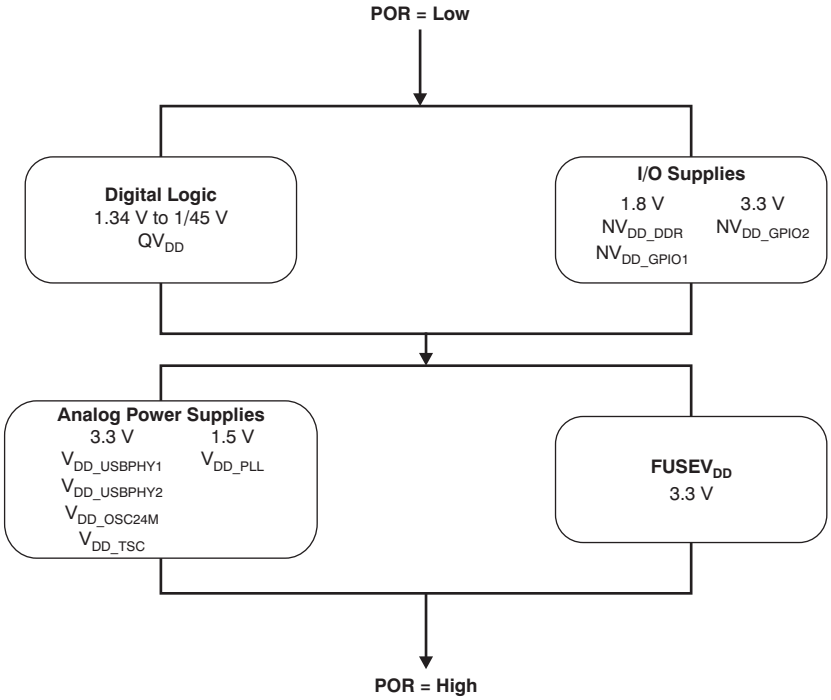

Figure 1. Recommended Power-Up Sequence

2.1.2 Power-Down Sequencing

The power-down sequence has no special requirements.

3 Powering Freescale i.MX25 with the TPS65051: Reference Design

The TPS65051 is an integrated power management device, suitable for applications that require multiple power rails. The TPS65051 provides two highly efficient, 2.25-MHz step-down converters as well as four low dropout (LDO) regulators. The block diagram of the TPS65051 is shown in Figure 2.

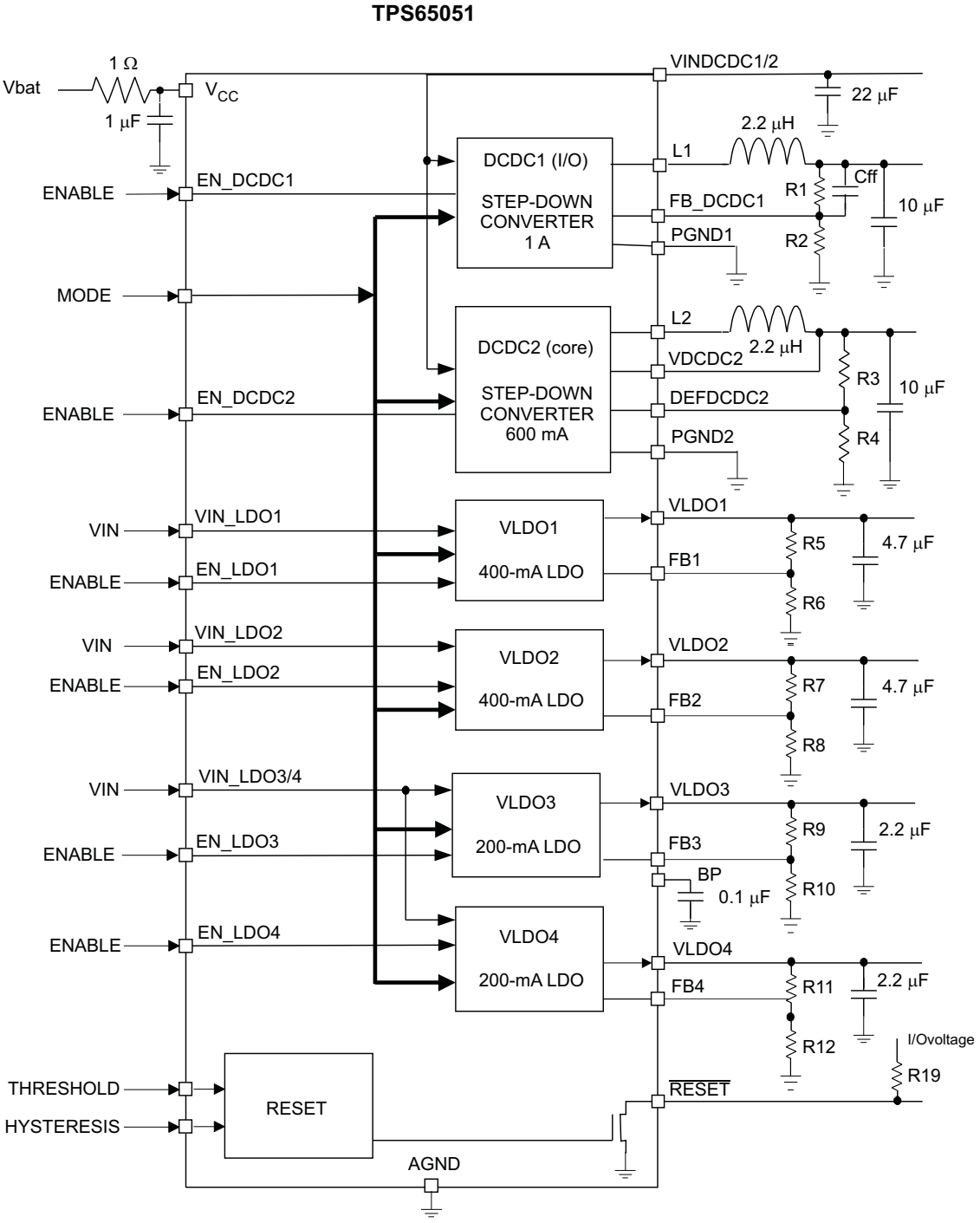

Figure 2. TPS65051 PMU Block Diagram

Following the pattern shown in Figure 1, a power-up sequence that consists of two groups was configured and applied in the power reference design conceived for this report.

The first group in the power-up sequence consists of all rails supplied by DCDC1, DCDC2, and the LDO LDO1. The second group contains LDO2, LDO3, and LDO4. Table 2 describes the converter output rail assigments for the TPS65051.

Table 2. TPS65051 Assignment of Converter Output Rails

Supply Rail		Voltage (V)	TPS65051 Output	Sequencing Order
QV_{DD}	Core	1.45	DCDC1	1
NV_{DD_GPIO1}, NV_{DD_GPIO2}, NV_{DD_SDRAM}		3.3	DCDC2	1
NV_{DD_MDDR}, NV_{DD_DDR2}		1.8	LDO1	1
$V_{DD\_USBPHY1}$, $V_{DD\_USBPHY2}$, V_{DD_OSC24M}, V_{DD_TSC}, V_{REF}		3.3	LDO2	2
$FUSEV_{DD}$		3.6	LDO3	2
V_{DD_PLL}		1.6	LDO4	2

Figure 3 illustrates the reference design schematic.

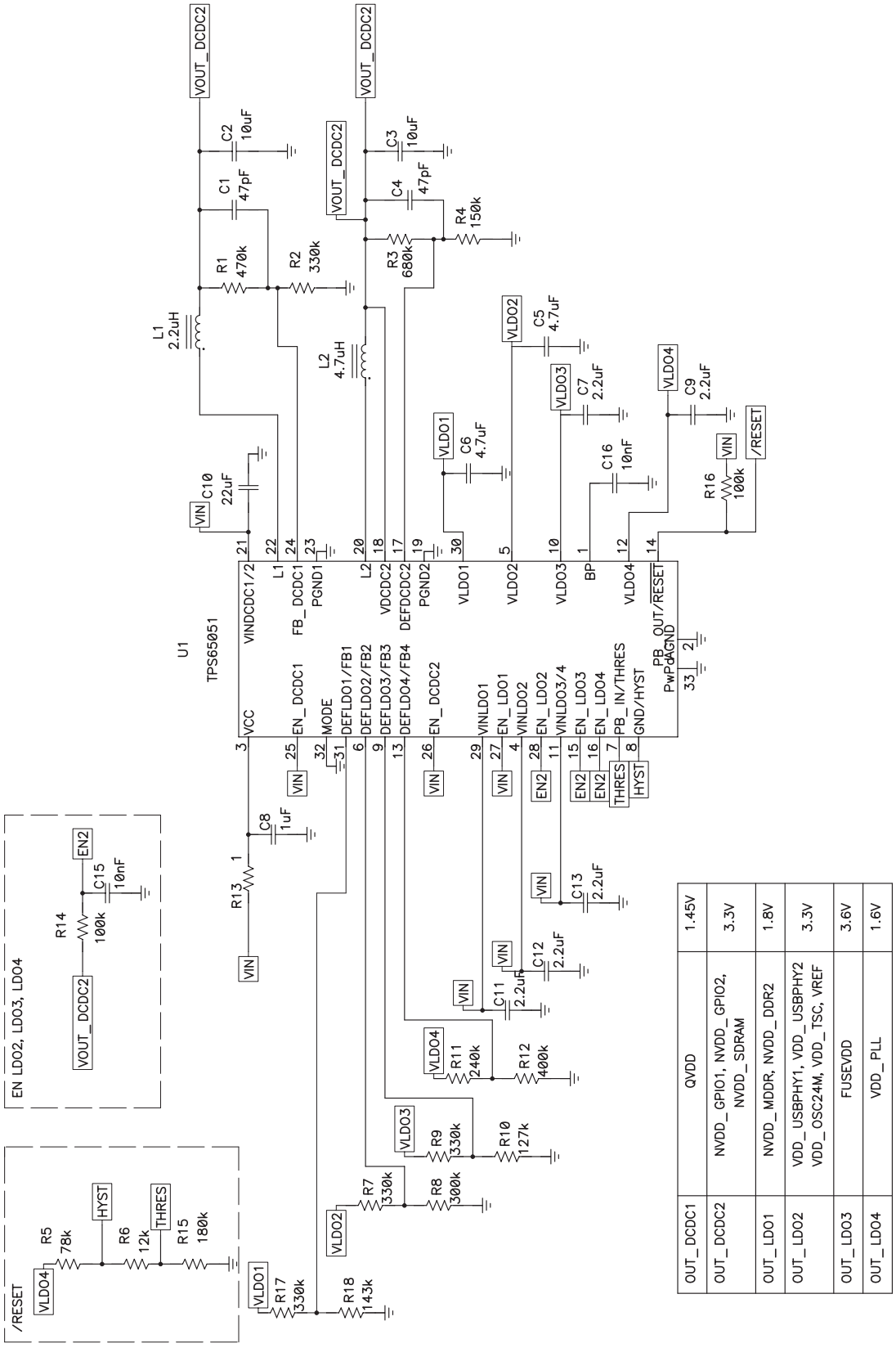

Figure 3. Reference Design Schematic

Table 3 provides the parts list for the reference design.

Table 3. List of Materials

Count	Ref Des	Value	Description	Size	Part No	Mfr
2	C1, C4	47 pF	Capacitor, ceramic, 50V, COG, 5%	0603	C1608C0G1H470J	TDK
1	C10	22 µF	Capacitor, ceramic, 6.3 V, X5R, 20%	0805	GRM21BR60J226ME39L	Std
2	C15, C16	10 nF	Std	0805	Std	muRata
2	C2, C3	10 µF	Capacitor, ceramic, 10 V, X5R, 20%	0805	GRM188R60J106ME47D	muRata
2	C5, C6	4.7 µF	Capacitor, ceramic, 10 V, X5R, 10%	0805	GRM21BR61A106KE19L	muRata
5	C7, C9, C11, C12, C13	2.2 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	GRM188R60J225KE01D	muRata
1	C8	1 µF	Capacitor, ceramic, 25 V, X5R, 10%	0805	GRM188R61E105KA12D	muRata
1	L1	2.2 µH	Inductor, SMT, 1.3 A, 130 mΩ	0.118 x 0.118 inch	LPS3015-332ML	Coilcraft
1	L2	4.7 µH	Inductor, SMT, 1.3 A, 130 mΩ	0.118 x 0.118 inch	LPS3015-332ML	Coilcraft
1	R1	470 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R10	127 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R11	240 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R12	400 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R13	1 Ω	Resistor, chip, 1/16W, 1%	0603	Std	Std
2	R14, R16	100 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R15	180 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R18	143 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
4	R2, R7, R9, R17	330 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R3	680 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R4	150 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R5	78 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R6	12 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R8	300 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS65051	IC, 2.25-MHz Dual Step-Down Converter with Four Low-Input Voltage LDOs	QFN-32	TPS65050/51	TI

4 Detailed Design Information

QV_{DD} (1.45 V)

This rail is supplied by DCDC1.

The output voltage of DCDC1 is adjustable using an external voltage divider. Using Equation 4 from the TPS65051 data sheet, for an output voltage of 1.45 V, the external voltage divider values can be calculated as shown:

R1 = 470 kΩ, R2 = 330 kΩ, C_{FF} = 47 pF

QVDD is part of the first sequencing group. Therefore, the EN DCDC1 pin can be directly connected to VIN.

NV_{DD_GPIO1}, NV_{DD_GPIO2}, NV_{DD_SDRAM} (3.3 V)

This rail is supplied by DCDC2.

The output voltage of DCDC2 is also adjustable using an external voltage divider. Using Equation 5 from the TPS65051 data sheet, for an output voltage of 3.3 V, the external voltage divider values can be calculated in the following way:

R3 = 680 kΩ, R4 = 150 kΩ, C_{FF} = 47 pF

The rails NVDD_GPIO1, NVDD_GPIO2, and NVDD_SDRAM are part of the first sequencing group. EN DCDC2 can thus be directly connected to VIN.

NV_{DD_MDDR}, NV_{DD_DDR2} (1.8 V)

These rails are supplied by LDO1.

The output voltage of LDO1 is adjustable using an external voltage divider. Using Equation 9 from the TPS65051 product data sheet, for an output voltage of 1.8 V, the external voltage divider values can be calculated in this way:

R5 = 240 kΩ, R6 = 300 kΩ

The rails NVDD_MDDR and NVDD_DDR2 are part of the first sequencing group. EN LDO1 can be directly connected to VIN.

$V_{DD\_USBPHY1}$, $V_{DD\_USBPHY2}$, V_{DD_OSC24M}, V_{DD_TSC}, V_{REF} (3.3 V)

These rails are supplied by LDO2.

The output voltage of LDO2 is adjustable using an external voltage divider. Using Equation 9 from the TPS65051 product data sheet, for an output voltage of 3.3 V, the external voltage divider values can be calculated as shown:

R17 = 330 kΩ, R18 = 143 kΩ

The rails $V_{DD\_USBPHY1}$, $V_{DD\_USBPHY2}$, V_{DD_OSC24M}, V_{DD_TSC}, and V_{REF} are part of the second sequencing group. EN LDO2 is connected to the output of DCDC2. In addition there is an RC filter connected on EN LDO2 to make sure the second sequencing groups starts after DCDC2.

Generation of $FUSEV_{DD}$ (3.6 V)

These rails are supplied by LDO3.

The output voltage of LDO3 is adjustable using an external voltage divider. Using Equation 9 from the TPS65051 data sheet, for an output voltage of 3.6 V, the external voltage divider values can be calculated as following

R9 = 470 kΩ, R10 = 180 kΩ

The rail $FUSEV_{DD}$ is part of the second sequencing group. EN LDO3 is connected to the output of DCDC2. In addition, there is an RC filter connected on EN LDO3 to ensure that the second sequencing groups starts after DCDC2.

Generation of V_{DD_PLL} (1.6 V at 200 mA)

These rails are supplied by LDO4.

The output voltage of LDO4 is adjustable using an external voltage divider. Using Equation 9 from the TPS65051 product data sheet, for an output voltage of 1.6 V, the external voltage divider values can be calculated as shown:

R11 = 220 kΩ, R12 = 360 kΩ

The rail $FUSEV_{DD}$ is part of the second sequencing group. EN LDO4 is connected to the output of DCDC2. In addition, there is an RC filter connected on EN LDO4 to make sure the second sequencing groups starts after DCDC2.

POR

The reset signal for the processor is generated using the integrated SVS onboard the TPS65051 PMU. The SVS monitors the last rail coming up in the power sequence. The last rail is OUT_LDO4 (that is, VDD_PLL). In the design, this rail is monitored; once it reaches 0.3 V, the RESET signal is generated.

5 Measurement Results

This section presents some of the measured performance results for this configuration.

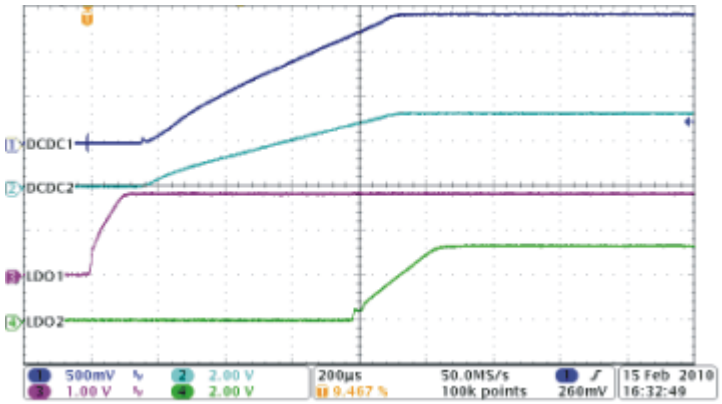

Figure 4. Power-Up Sequence: DCDC1, DCDC2, LDO1, LDO2

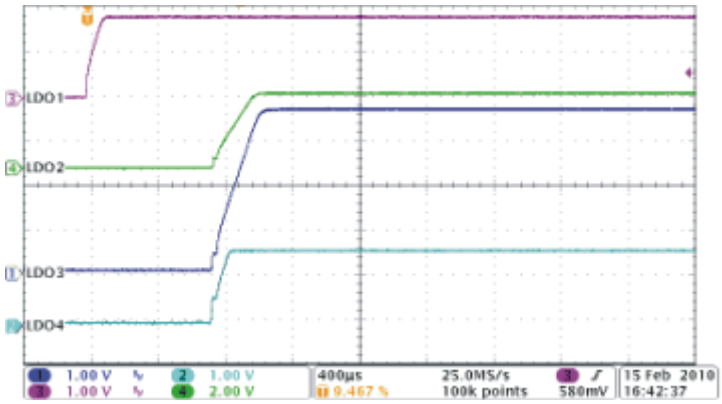

Figure 5. Power-Up Sequence: LDO1, LDO2, LDO3, LDO4

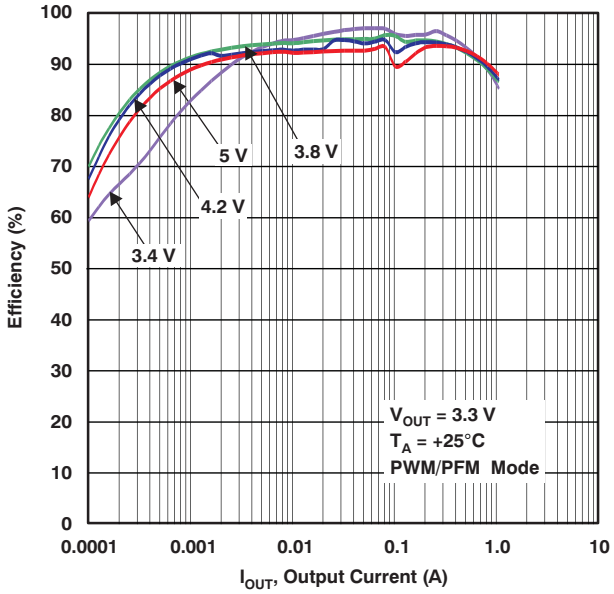

Figure 6. Efficiency (DCDC1)

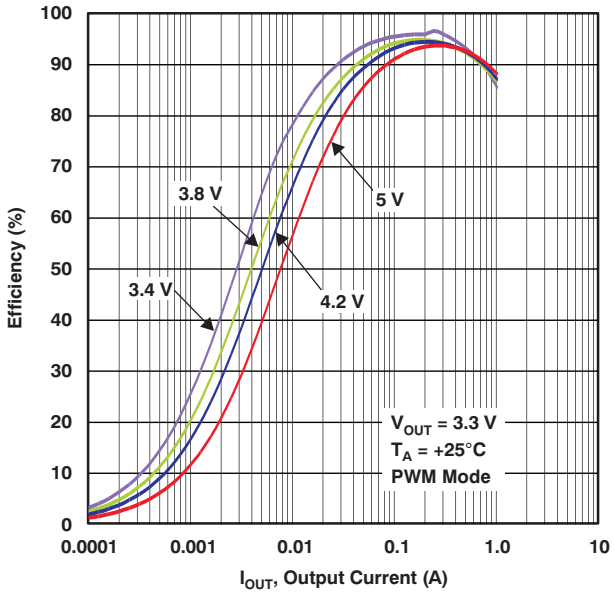

Figure 7. Efficiency (DCDC2)

6 References

1. i.MX25 Power Management Using the MC34704. (2009). Application note AN3820. Freescale Semiconductor, Inc.
2. TPS65051 product data sheet. Texas Instruments (SLVS710A). Revised August, 2007.

Revision History

Changes from Original (February, 2010) to A Revision	Page
• Updated Figure 3	6
• Replaced Bill of Materials	7
• Corrected resistor names indicated is calculation of external voltage divider value	8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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