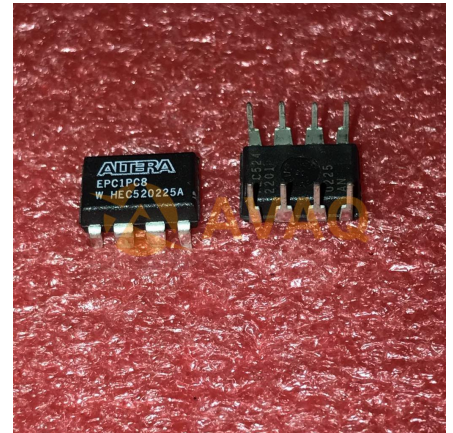


## Configuration SRAM for FBGA

<b>Manufacturer:</b>	<a href="#">Intel Corp</a>
<b>Package/Case:</b>	DIP8
<b>Product Type:</b>	Programmable Logic ICs
<b>Lifecycle:</b>	Obsolete



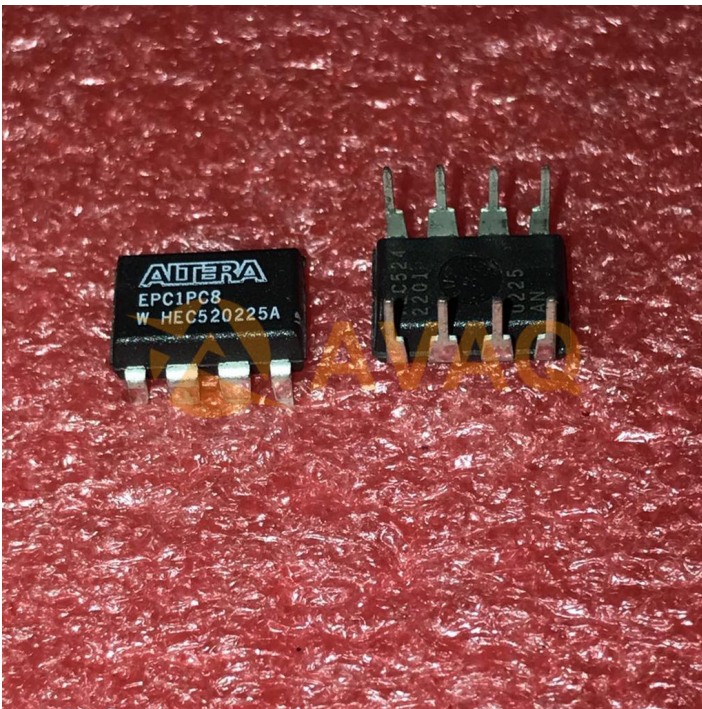
Images are for reference only

[Inquiry](#)

## General Description

The MAX 9000 family of in-system-programmable, high-density, high-performance EPLDs is based on Altera's third-generation MAX architecture. Fabricated on an advanced CMOS technology, the EEPROMbased MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 10 ns, and counter speeds of up to 144 MHz.

High-performance CMOS EEPROM-based programmable logic devices (PLDs) built on third-generation Multiple Array Matrix (MAX®) architecture



## Recommended For You

**EPMB256AQC208-10N**

Intel Corp

QFP208

**EPCQ32ASI8N**

Intel Corp

SOP8

**EPCQ32SI8N**

Intel Corp

SOP8

**EPCQ64ASI16N**

Intel Corp

SOP16

**EPCQ16SI8N**

Intel Corp

SOP8

**EPC2H32**

Intel Corp

QFP

**EPM7128STC100-15N**

Intel Corp

QFP100

**EP1C6Q240I7N**

Intel Corp

QFP240

**EPCQ128SI16N**

Intel Corp

SOP16

**EPM7128SLC84-15N**

Intel Corp

PLCC

**EPC1213PC8**

Intel Corp

DIP8

**EP1K30TC144-3N**

Intel Corp

QFP

**EPCS1SI8**

Intel Corp

SOP-8

**EPC1PI8N**

Intel Corp

DIP8

**EPC2LI20N**

Intel Corp

PLCC