AD9515BCPZ-REEL7

Clock Divider Buffer 2-OUT 1-IN 1:2 32-Pin LFCSP EP T/R

Manufacturer:	Analog Devices, Inc
Package/Case:	LFCSP-32
Product Type:	Drivers
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

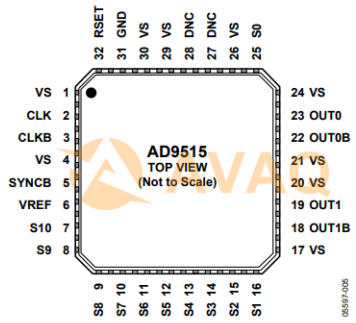

Figure 6. 32-Lead LFCSP Pin Configuration

Images are for reference only

Inquiry

General Description

The AD9515 features a two-output clock distribution IC in a design that emphasizes low jitter and phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements also benefit from this part.

There are two independent clock outputs. One output is LVPECL, while the other output can be set to either LVDS or CMOS levels. The LVPECL output operates to 1.6 GHz. The other output operates to 800 MHz in LVDS mode and to 250 MHz in CMOS mode.

Each output has a programmable divider that can be set to divide by a selected set of integers ranging from 1 to 32. The phase of one clock output relative to the other clock output can be set by means of a divider phase select function that serves as a coarse timing adjustment.

The LVDS/CMOS output features a delay element with three selectable full-scale delay values (1.5 ns, 5 ns, and 10 ns), each with 16 steps of fine adjustment.

The AD9515 does not require an external controller for operation or setup. The device is programmed by means of 11 pins (S0 to S10) using 4-level logic.

The programming pins are internally biased to ⅓ VS. The VREF pin provides a level of ⅔ VS. VS (3.3 V) and GND (0 V) provide the other two logic levels.

The AD9515 is ideally suited for data converter clocking applications where maximum converter performance is achieved by encode signals with subpicosecond jitter.

The AD9515 is available in a 32-lead LFCSP and operates from a single 3.3 V supply. The temperature range is −40°C to +85°C.

Key Features

1.6 GHz differential clock input

2 programmable dividers, in range from 1 to 32 Phase select for output-to-output coarse delay adjust

1.6 GHz LVPECL clock outputLVPECL Additive output jitter 225 fs rms

800 MHz/250 MHz LVDS/CMOS clock outputLVDS/CMOS Additive output jitter 300 fs rms/290 fs rmsTime delays up to 10 ns

Device configured with 4-level logic pins

Space-saving, 32-lead LFCSP

Application

Low jitter, low phase noise clock distribution

Clocking high speed ADC, DAC, DDS, DDC, DUC, MxFE

High performance wireless transceivers

High performance instrumentation

Broadband infrastructure

ATE

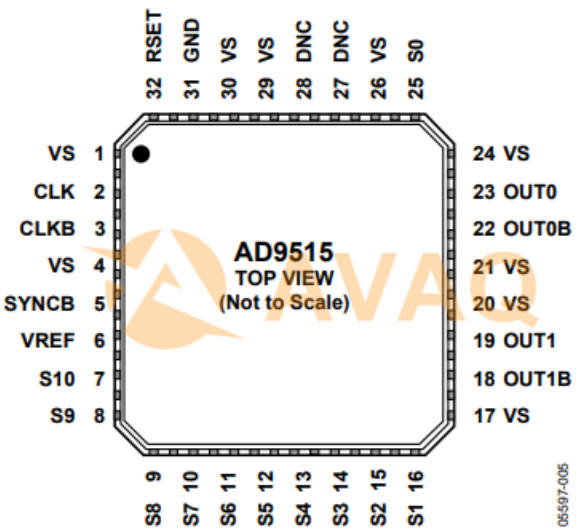

Figure 6. 32-Lead LFCSP Pin Configuration

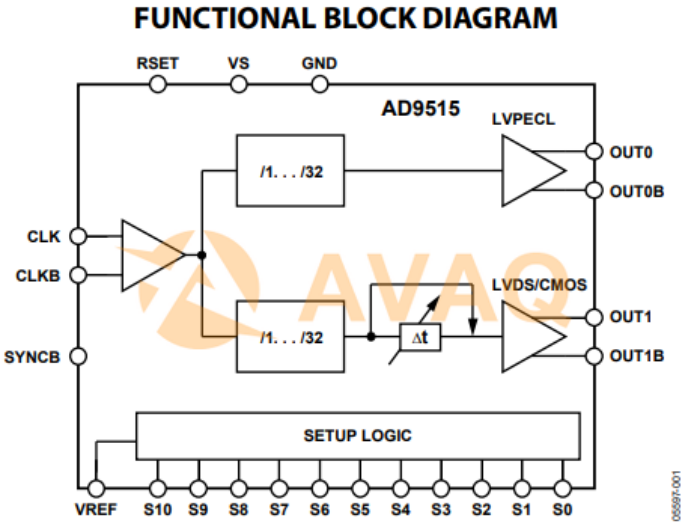

Figure 1.

Recommended For You

AD9517-3ABCPZ
Analog Devices, Inc
QFN

AD9954YSV
Analog Devices, Inc
QFP

ADCLK914BCPZ-WP
Analog Devices, Inc
LFCSP-16

AD7008JP50
Analog Devices, Inc
PLCC44

AD9952YSV
Analog Devices, Inc
QFP

AD9516-3BCPZ
Analog Devices, Inc
QFN

ADCLK944BCPZ-R2
Analog Devices, Inc
LFCSP16

AD9577BCPZ
Analog Devices, Inc
LFCSP-40

AD9543BCPZ
Analog Devices, Inc
LFCSP-48

AD9853AS
Analog Devices, Inc
QFP

ADN2805ACPZ
Analog Devices, Inc
LFCSP

ADN2807ACPZ
Analog Devices, Inc
48-LFCSP

AD9520-4BCPZ
Analog Devices, Inc
LFCSP

AD9831AST
Analog Devices, Inc
QFP

ADN2855ACPZ
Analog Devices, Inc
LFCSP32