MAX2769/MAX2769C PLL Loop Filter Calculator User Guide

UG6444; Rev 0; 6/17

Abstract

This document briefly covers PLL basics and explains how to use the PLL loop filter spreadsheet calculator for the MAX2769/MAX2769C. The calculator allows users to design and implement the loop filter values specific to their application.

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1. Introduction

The MAX2769 and MAX2769C are next-generation Global Navigation Satellite System (GNSS) receivers covering L1/E1, B1, G1 bands for GPS, Galileo, BeiDou, and GLONASS satellite systems on a single chip. These single-conversion GNSS receivers are designed to provide high performance for industrial applications and a wide range of consumer applications, including mobile handsets.

The MAX2769/MAX2769C include an integrated VCO, a crystal oscillator, and a fractional-N frequency synthesizer to program the LO frequency using different reference input frequencies.

A spreadsheet calculator for PLL loop filter design has been developed and is downloadable from the IC QuickView webpage under Design Resources. This user guide explains in detail how to work with the calculator.

2. Back to Basics: Phase-Locked Loops

Figure 1 shows the blocks included in a typical PLL.

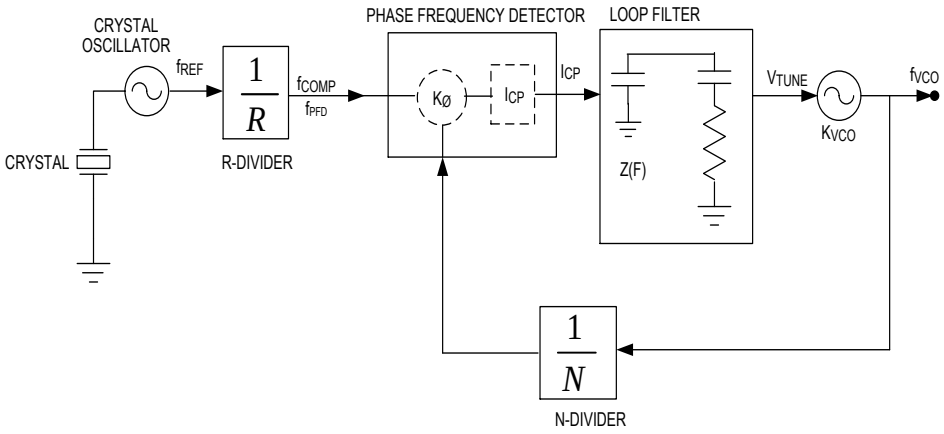

Figure 1. Block diagram of a typical PLL.

- The reference crystal oscillator frequency, f_{REF}, is divided by using R-Divider to produce the comparison frequency (f_{COMP}), which is also called the phase frequency detector (PFD) frequency.
- The VCO frequency, f_{VCO}, is divided to produce the same f_{COMP} frequency by using N-divider.
- The PFD compares the frequency and phase difference between f_{VCO}/N and f_{REF}/R. The charge pump (CP) generates current pulses proportional to the mismatch.
- The loop filter smoothens and integrates the error signal to produce a DC voltage to tune the VCO in the direction to eliminate the error in phase and frequency.

Based on the implementation of the N-divider, the PLLs can be divided into integer-N or fractional-N types, each of which have their own advantages and disadvantages. Deeper discussion of fractional-N PLLs is outside the scope of this document.

3. Phase Noise in PLLs

Phase noise is a measure of short-term frequency deviation from the ideal frequency due to random phase fluctuation, also called jitter in the time domain. It is defined as the ratio of power measured in a 1Hz bandwidth at a known offset to the total carrier power and is specified of units of dBc/Hz. It is customary to characterize an oscillator in terms of its single-sideband phase noise as shown in Figure 2.

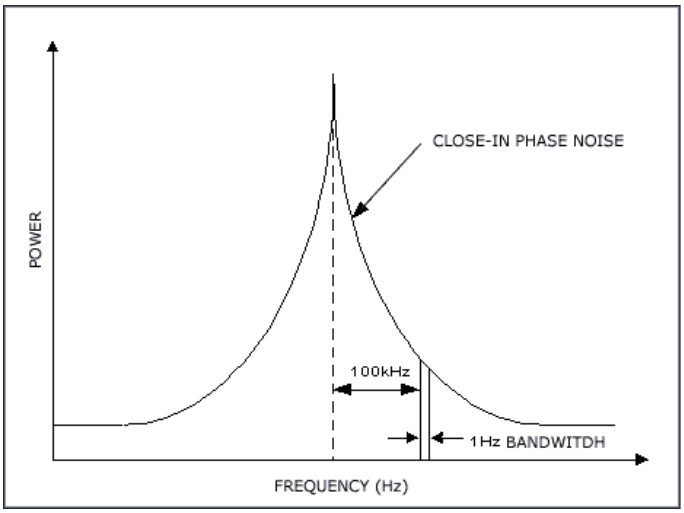

Figure 2. Phase noise plot.

3.1. Phase Noise Contributions from Different Blocks

- Phase noise inside the loop filter bandwidth is a combination of phase noise contributed by the reference input, PLL, and VCO.
- The PLL noise contributors are the charge pump, PFD, and dividers.
- Phase noise is dominated by the VCO noise outside the loop bandwidth.
- VCO phase noise is highpass filtered by the closed-loop PLL response.
- All other noise sources are lowpass filtered and are multiplied by N.

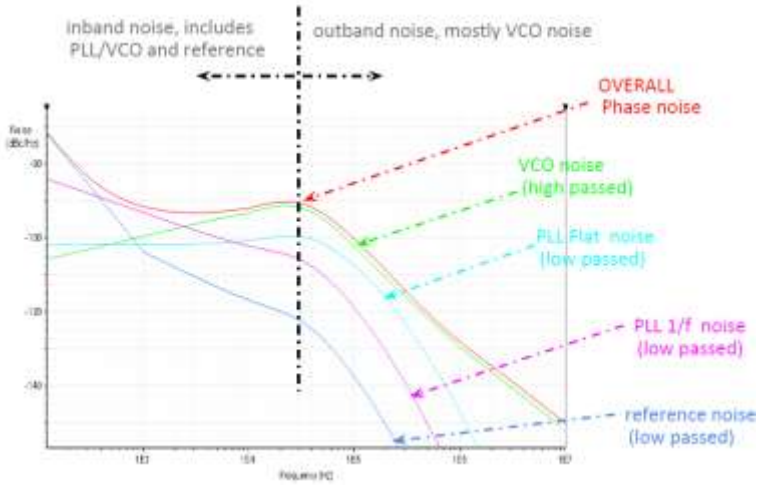

Figure 3. Phase noise contributions from different blocks.

4. Loop Filter

The loop filter integrates and filters the current pulses from the charge pump to generate the required VCO tuning voltage. The higher the loop filter order, the better the suppression of f_{COMP} related spurs.

The loop filter can be passive or active depending on the Vcc of the PLL device that should drive the VCO tuning voltage.

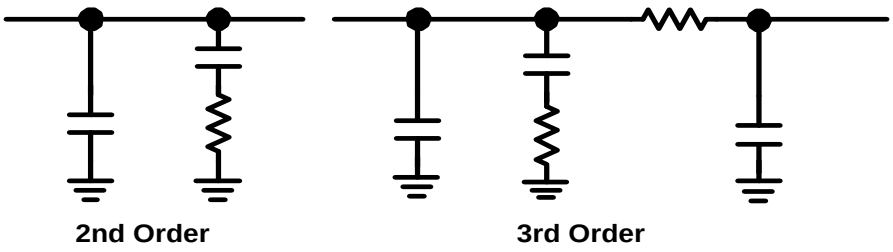

Figure 4. Different order loop filters.

The loop filter design is critical to get the desired performance from the PLL, as there are many trade-offs between the design specifications that need to be met.

4.1. Design Considerations

- PFD Frequency: The higher the PFD frequency, the lower the N-divider value is and the better the phase noise, as it is directly proportional to the N-divider value, (20 x log (N)).
- Lock Time: Time it takes to lock from one specified frequency to another specified frequency within a given frequency tolerance.
- Loop Bandwidth: Lowpass filter bandwidth that is achieved from the filter components.
    - The wider the loop bandwidth, the faster the lock time, but the trade-off is worse spurious performance.
    - The narrower the loop bandwidth, the better the spurious performance, but the lock time increases.
- PLL Stability: In theory, a phase margin of 0 degrees or less in the PLL open-loop response results in an unstable PLL.
    - A rule of thumb is that 45 degrees is generally the minimum required phase margin.

5. How to Work with the MAX2769/MAX2769C Loop Filter Spreadsheet Calculator

5.1. Overview

The loop filter spreadsheet calculator models the PLL as a linear model in the phase domain and is used to calculate the loop filter values and further simulate the phase noise.

The loop filter is a third-order passive filter with one of the poles determined by a resistor and capacitor within the IC. The remaining components in the filter are external with the values designated as c1, r2, c2.

All cells highlighted in light yellow are inputs and cells in white are outputs derived based on relevant formulae and are not supposed to be changed.

5.2. Inputs Control (Cells Highlighted in Light Yellow)

Respective step numbers are highlighted in the GUI snapshot figures.

1. The MAX2769/MAX2769C have an integrated VCO so the phase noise of the VCO is fixed and cannot be controlled.
2. Xtal model can be selected from three options named xtal1, xtal2, and ideal.
3. The phase noise of reference input can be entered as explained.
4. The reference input frequency can be entered under the cell ref(MHz), as shown in Figure 5. It ranges from 8MHz to 32MHz.
5. The R-divider value can be entered and it ranges from 1 to 1023.
6. Charge pump current, CP(mA), can be selectable as either 0.5mA or 1mA.
7. outA(MHz) is the desired output from the PLL that varies from 1550MHz to 1610MHz.

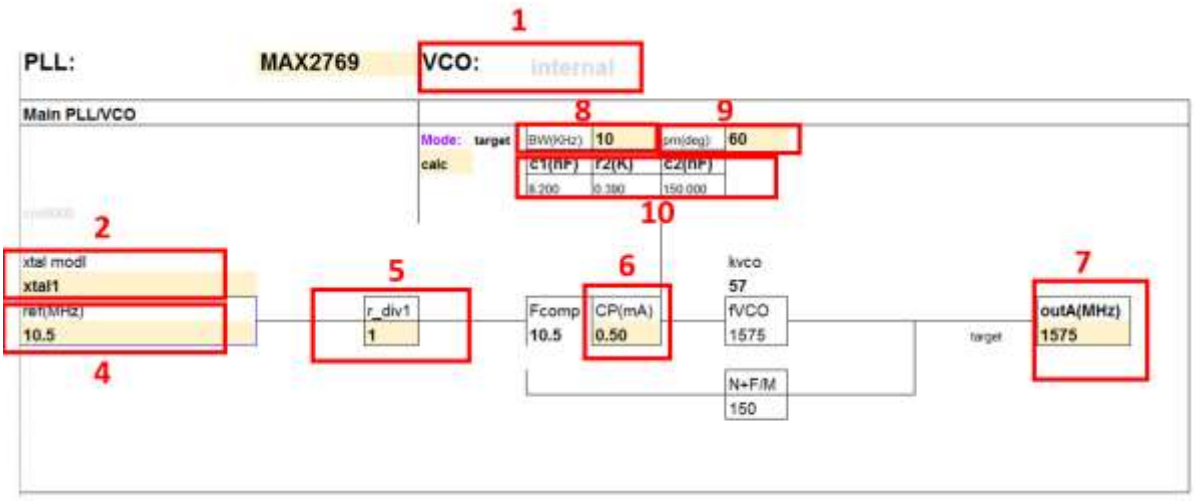

Figure 5. Loop filter spreadsheet calculator.

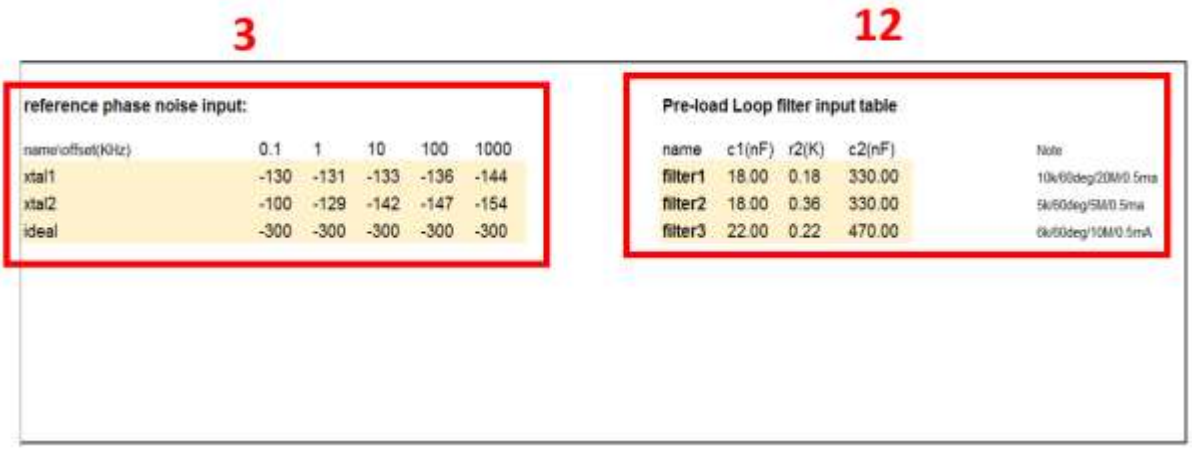

Figure 6. Loop filter spreadsheet calculator: Steps 3 and 12.

8. Enter the desired loop bandwidth under the BW(KHz) cell.
9. Enter the desired phase margin value under the pm(deg) cell.
10. Once all the required inputs are entered, set the Mode to calc and the user can see the loop filter values calculated and displayed under cells c1(nF), r2(K), and c2(nF)
11. The user has an option to simulate the phase noise with pre-loaded values by selecting freeze under Mode.
12. Also, the user can enter pre-loaded loop filter values (filter1, filter2, filter3) and see the phase noise simulation results by selecting freeze under Mode.
13. Based on the parameters and loop filter values calculated, the phase noise is simulated and shown in Figure 7.

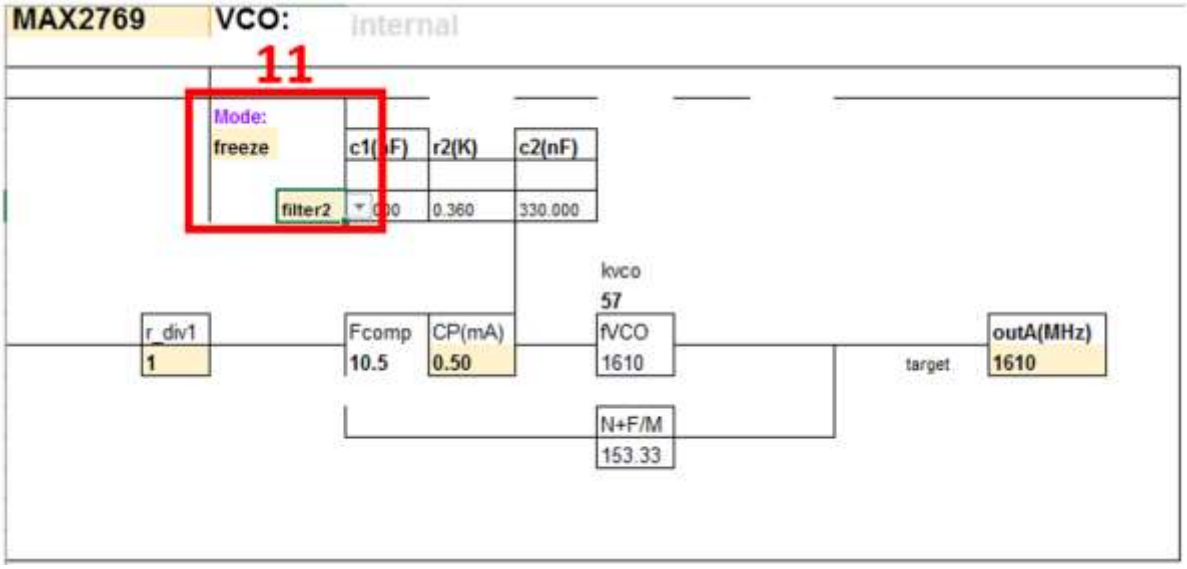

Figure 7. Loop filter spreadsheet calculator mode.

5.3. Understanding the Simulation Results

1. Phase noise contribution from different blocks and the total closed-loop phase noise has been plotted.
2. Achieved loop bandwidth and phase margin are displayed.
3. Integration limits can be changed via the LL(KHz) and HL(KHz) cells.
4. Based on the integration limits, different parameters such as SSB phase noise (dB-SSB), DSB phase noise (dB-DSB), phase noise in degrees (deg), mrad, RMS jitter (ps), and FM(KHz) can be calculated.

The user can observe the phase noise at the desired offsets as shown in

5. Figure *8*.
6. Loop filter cutoff bandwidth with the calculated values is plotted.
7. Open loop gain and phase (Open loop Gain/Phase) is also plotted.

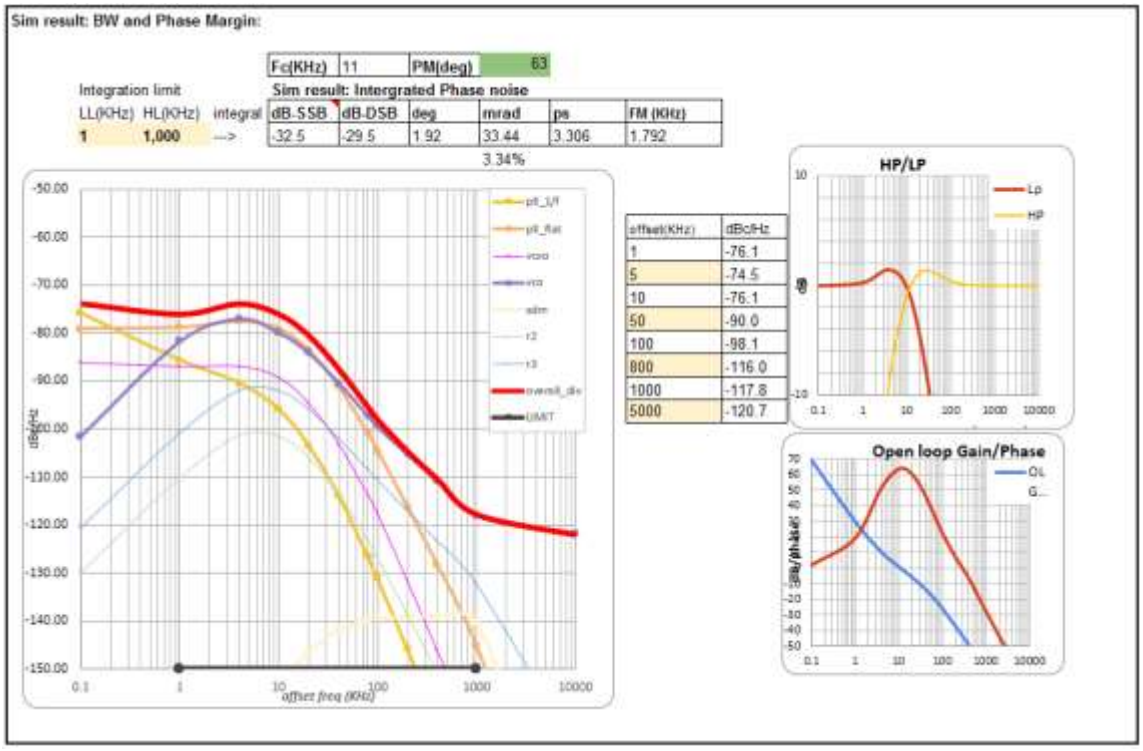

Figure 8. Simulation results.