AN2817
Application note

Guidelines for application design using L5962

Introduction

L5962 is a multi-regulator especially intended for high-end automotive car-radio applications.

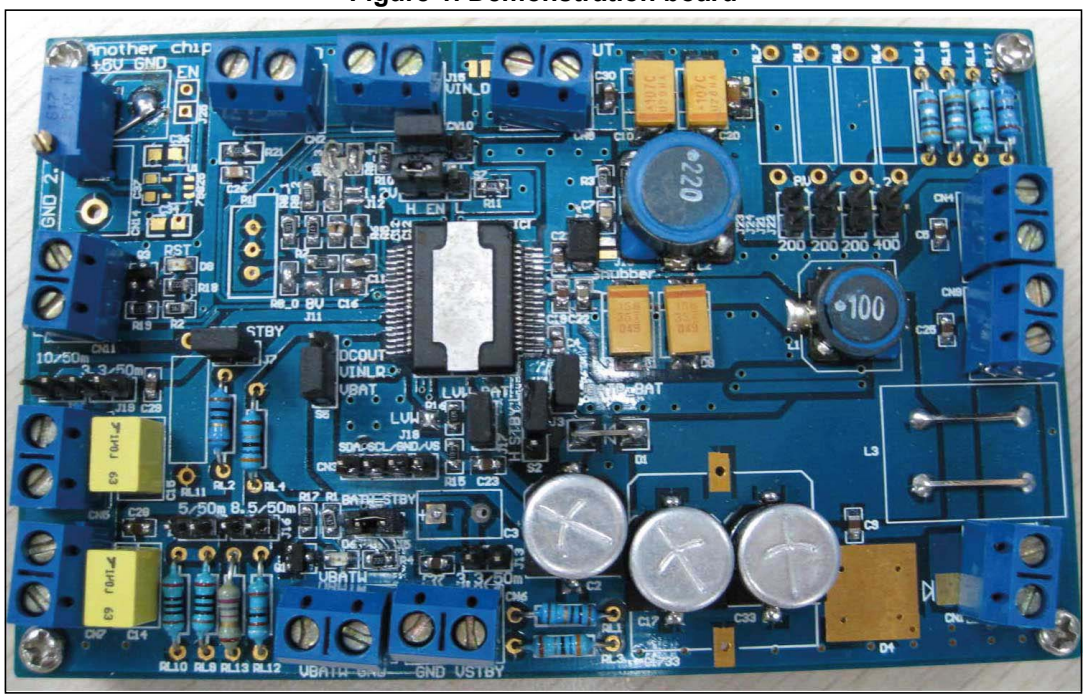
L5962 integrates 3 linear voltage regulators, 2 high side drivers and a switching regulator to provide complete car-radio system control. It has an extremely low quiescent current in standby mode of operation, that guarantees a proper supply to the microcontroller even with the system in 'sleep' condition.

3 regulators are VSTBY, VLR1 and VLR2. VSTBY is a 3.3 V/5 V stand-by linear regulator with 150 mA maximum current capability. VLR1 is a 5 V/8.5 V switched linear regulator able to deliver 350 mA. VLR2 is a 3.3 V/5.0 V/5.5 V/6.0 V/7.0 V/7.5 V/8.0 V/10.0 V switched linear regulator with 1 A load current capability. The output voltages of VLR1 and VLR2 are configurable with I^2C bus.

Device embeds also 2 high side drivers (HSD1/2) that can be activated/deactivated through I^2C bus.

Additional features provided by the L5962 are: reset function, load dump protection, thermal shutdown, under voltage detection and over current limitation for every block.

Figure 1. Demonstration board



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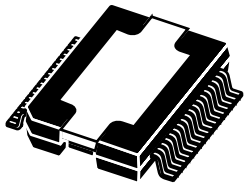
1 Pins function

Figure 2. PowerSO36 (slug up) outline drawing



GADG2406160831PS

Figure 3. Pin connection (top view)

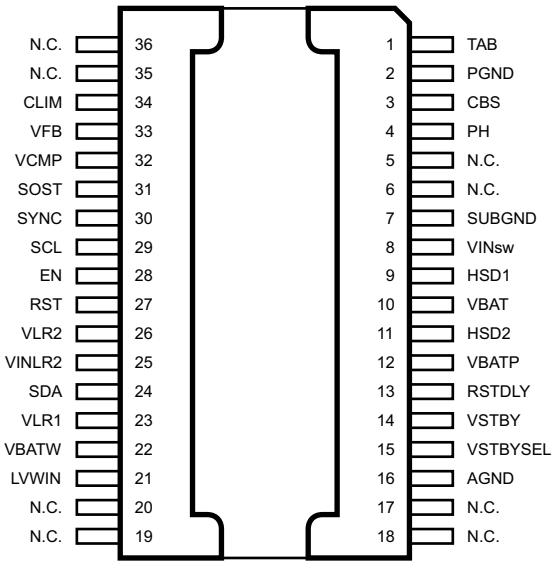


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Table 1. Pin connection

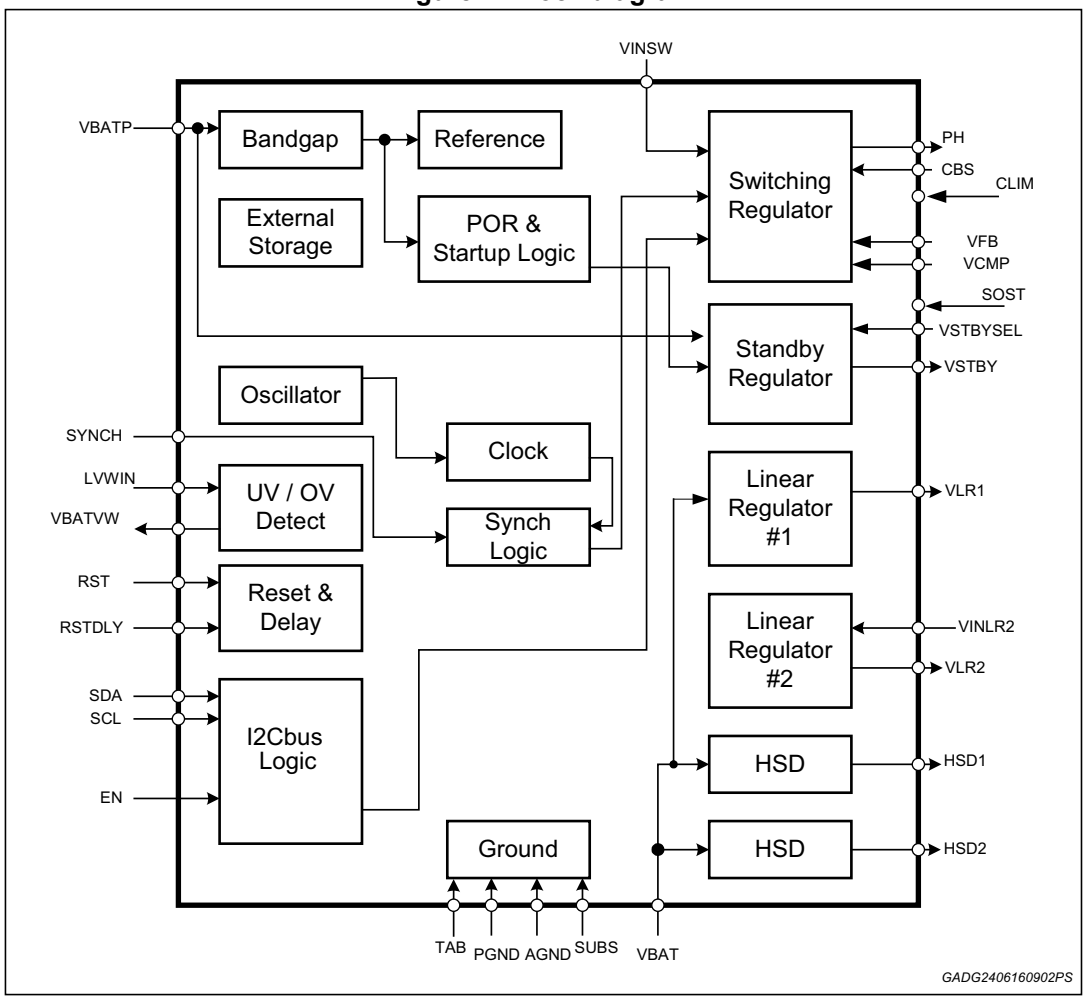
Pin #	Pad Name	Function
1	TAB	-
2	PGND	Switching regulator ground
3	CBS	Bootstrap for switching regulator
4	PH	Switching stage output
5	N.C.	Not connected
6	N.C.	Not connected
7	SUBGND	Substrate ground
8	VINsw	Switching regulator supply voltage
9	HSD1	High Side Driver 1
10	VBAT	VLR1/HSD1/HSD2 supply voltage
11	HSD2	High Side Driver 2

Table 1. Pin connection (continued)

Pin #	Pad Name	Function
12	VBATP	Stand-by regulator supply voltage
13	RSTDLY	Reset delay function
14	VSTBY	Stand-by regulator output
15	VSTBYSEL	Stand-by regulator selector
16	AGND	Analog ground
17	N.C.	Not connected
18	N.C.	Not connected
19	N.C.	Not connected
20	N.C.	Not connected
21	LVWIN	Battery detector adjustment input
22	VBATW	Battery detector output (open-drain)
23	VLR1	Switched linear regulator 1
24	SDA	I^2C bus DATA
25	VINLR2	VLR2 supply voltage
26	VLR2	Switched linear regulator 2
27	RST	Reset
28	EN	Enable
29	SCL	I^2C bus CLOCK
30	SYNC	Switching regulator SYNC function
31	SOST	Switching regulator soft-start
32	VCMP	Switching regulator compensation
33	VFB	Switching regulator feedback
34	CLIM	Switching regulator current limit selector
35	N.C.	Not connected
36	N.C.	Not connected

2 Block diagram

Figure 4. Block diagram



3 Functional description

The main internal blocks are shown in *Figure 4*, where is reported the device block diagram.

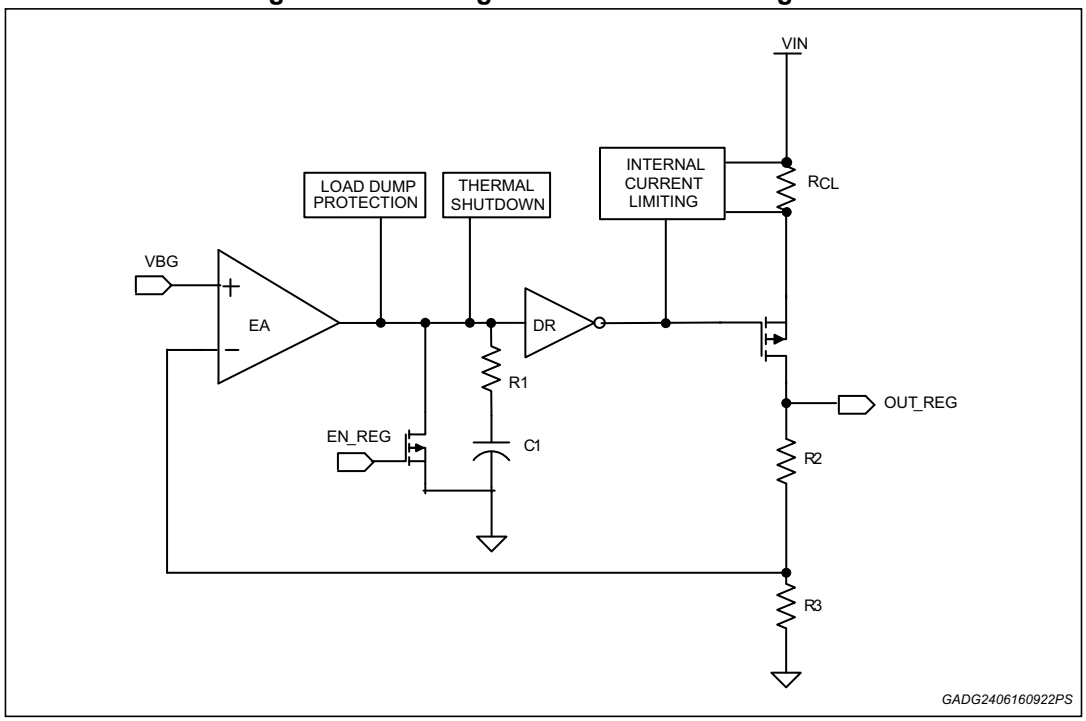
They are:

- One standby linear regulator (VSTBY)
- Two switched linear regulators selectable between 5/8.5 V (VLR1) and 3.3 V/5.0 V/ 5.5 V/ 6.0 V/7.0 V/7.5 V/8.0 V/10.0 V (VLR2) respectively
- One independent, adjustable, step-down, synchronous switching voltage regulator using internal DMOS transistors
- Synchronization function for switching regulator
- Soft-start control for switching regulator to protect external components from in-rush currents during turn-on
- Two protected, switched high-side drivers (HSD1, HSD2)
- VSTBY out-of-regulation detection with configurable delay (RST, RSTDLY)
- Battery voltage (under/over) warning output (VBATVW). Under-voltage threshold adjustable with external divider through dedicated pin
- I^2C interface for output voltage configuration of linear regulators and control functions
- Current-limit and independent thermal shutdown protection on all regulators and high side drivers
- Over-voltage detection and shutdown on all switched outputs
- Under-voltage lockout on low-voltage reset output

3.1 Linear regulators

Figure 5 shows the general block diagram of a linear regulator. It consists of Error Amplifier (EA), Driver (DR), Compensation Network, Load Dump Protection, Thermal Shutdown, Current Limiter and resistor divider for output level setting. The compensation consists of R1 and C1, whose introduce a zero in the transfer function to obtain enough Phase Margin in OUT_REG and thus guarantee loop stability. The output PMOS has a resistor in series at its Source terminal, R_{CL}: the current is sensed through R_{CL} and, if it reaches a predetermined threshold, the internal current limiting circuit will increase the gate voltage of power PMOS to clamp the output current.

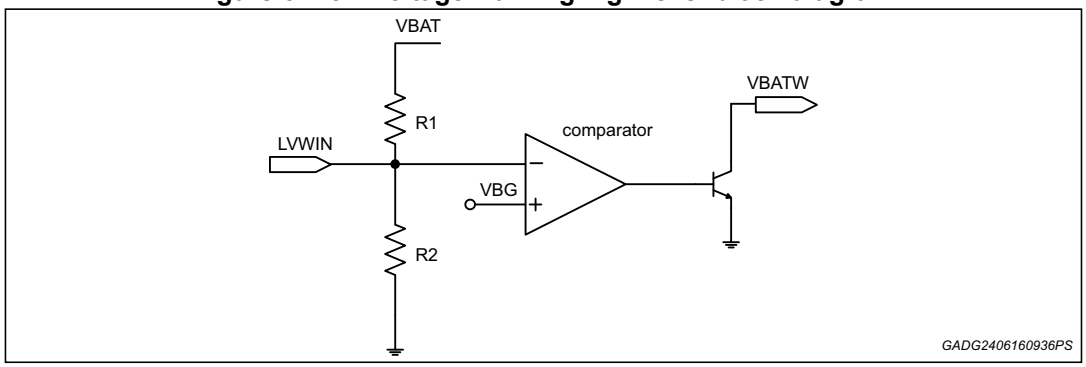
Figure 5. Linear regulator circuit block diagram



3.2 Low voltage warning

Figure 6 shows an high-level block diagram of low-voltage warning circuit. VBAT is divided by R1 and R2, whose values are internally fixed. When VBAT is decreasing so that LVWIN voltage gets lower than an internal reference (VBG) the comparator turns on the NPN transistor: VBATW is thus pulled down to ground, and warning is signaled.

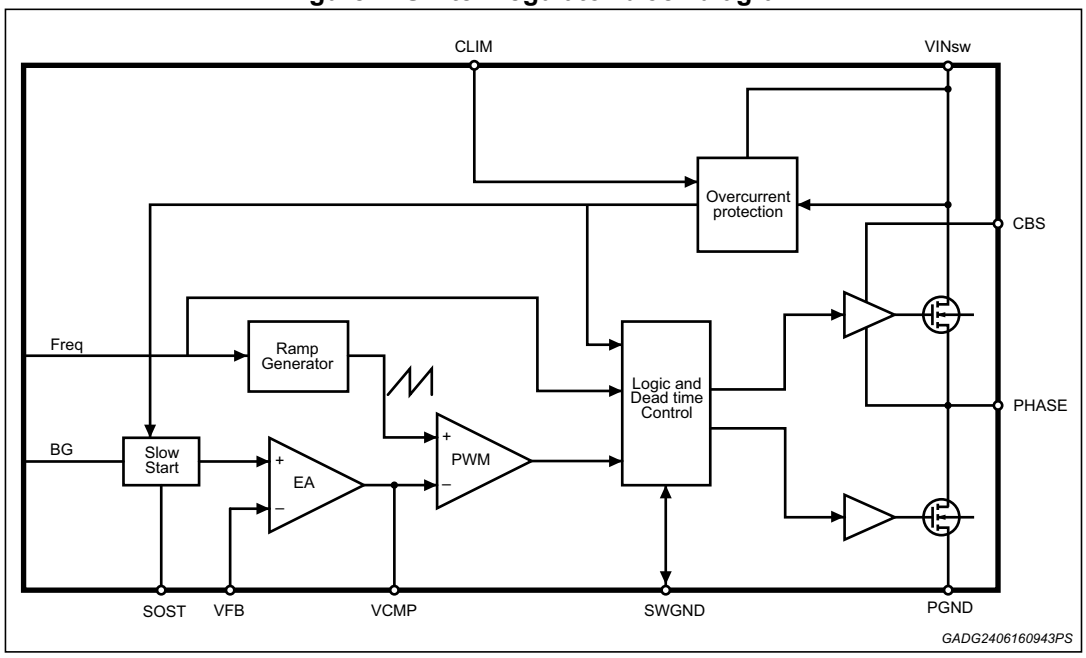
Figure 6. Low voltage warning high level block diagram



3.3 Switching regulator

L5962 switching regulator (shown in *Figure 7*) works in voltage mode. An error amplifier compares VFB and VBG and amplifies the difference, its output voltage is compared with the output of an internal Ramp Generator by a voltage comparator to produce the PWM signal. In the logic block other signals as Freq and the over current protection flag are elaborated along with PWM signal to control DC/DC behavior. The logic block output is provided to the drivers of high side NDMOS and low side NDMOS separately to drive the internal power switches.

Figure 7. Switch regulator block diagram



3.3.1 Soft-start

The soft-start block (Slow Start in*Figure 7*) protects external components from inrush current during switching regulator turn-on. Actually, soft-start function is realized by an internal resistor in series with an external capacitor, to obtain a low enough time constant for the turn-on transition.

3.3.2 Oscillator and synchronizer

Figure 8 shows the block diagram of the internal synchronizer.

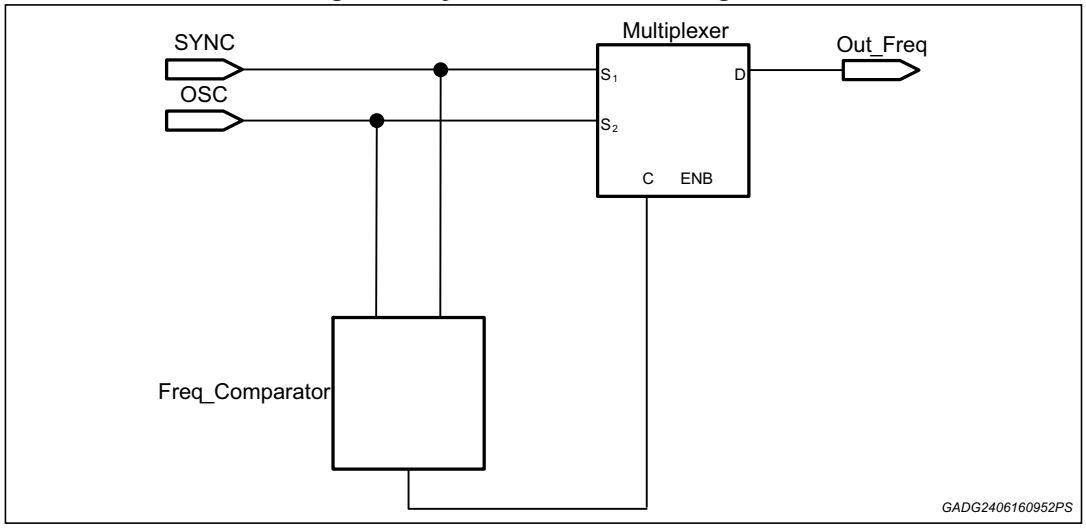
Oscillator provides the signal (OSC) that sets the switching frequency of the device, fixed at 200 kHz. SYNC represents the external frequency signal.

OSC and SYNC are compared by Freq_Comparator block: if the frequency of SYNC is higher than the one of OSC the Out_Freq of Multiplexer is equal to the frequency of SYNC and vice versa. Out_Freq signal is used as the PWM control signal and as the input of Ramp Generator.

User should take into account that SYNC signal can't be applied/disconnected/ quickly changed during regulator operation, otherwise a significant voltage transition may be generated on the regulated voltage due to the intrinsic relatively slow loop response

characterizing voltage mode DC/DC converters. Higher transients occur in particular in high Vout and high load current conditions.

Figure 8. Synchronizer block diagram



3.3.3 Current protection

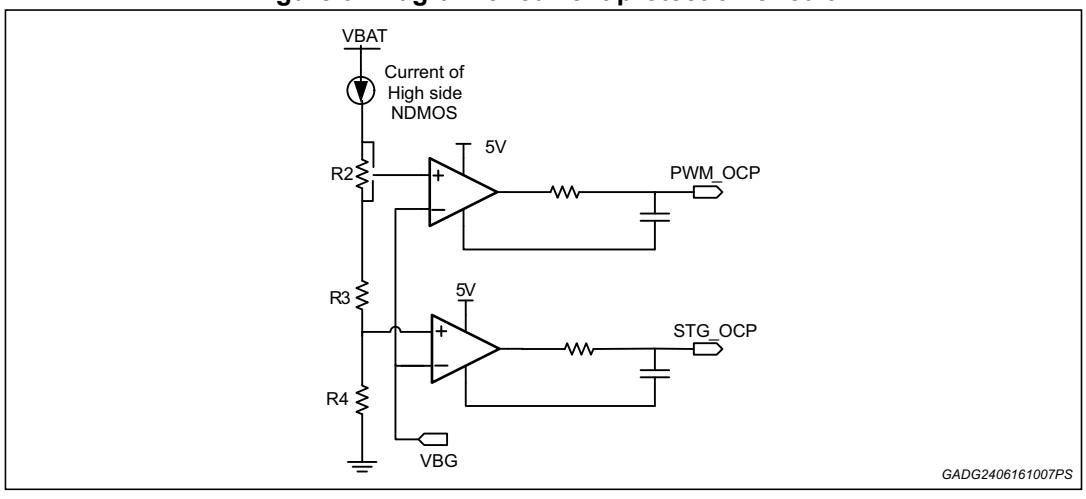
Switching regulator is equipped with two over current protection circuits (OCP), the former called PWM_OCP and the latter STG_OCP, which are shown in *Figure 9*.

When output current level is in normal range both PWM_OCP and STG_OCP output flags are low. When output current increase above a certain threshold (fixed by CLIM) PWM_OCP is pulled high: when this happens PH pin is forced to 0V, clamping duty-cycle value.

In extreme conditions like short circuit to ground of the output, PWM_OCP protection could be not enough: if current through high side NDMOS continued to increase even when PWM_OCP protection is operating, STG_OCP gets activated and turns immediately off the regulator, keeping it off for 8 periods.

STG_OCP threshold is ~2 A higher than the PWM_OCP one.

Figure 9. Diagram of current protection circuit

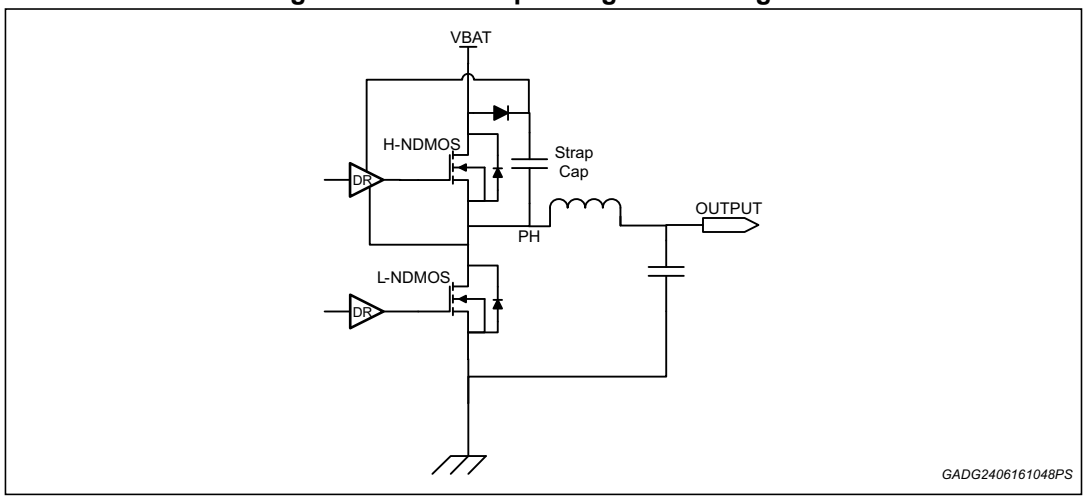


3.3.4 PWM output stage

Switching regulator output stage (shown in *Figure 10*) consists basically of two driver circuits, two NDMOS, a diode and a bootstrap circuit. In order to avoid shoot-through the two NDMOS can not be turned on at the same time: prior of turning on H-NDMOS drivers detect the gate voltage of L-NDMOS to verify it's effectively in OFF state. In the same way, before L-NDMOS is turned on drivers verify that H-NDMOS is in OFF state.

Thanks to the presence of bootstrap capacitor H-NDMOS gate is driven with a Vs + 10 V voltage and works in linear region with small output impedance.

Figure 10. PWM output stage block diagram



3.3.5 Thermal shutdown

Switching regulator embeds a thermal protection circuit that turns off the power stage if the local internal temperature of the chip gets higher than a fixed threshold (160 °C). The thermal shutdown signal is one of the input signals of Logic Block and thus influences directly the power stage control. The sensing element inside the chip is very close to the power NDMOS area ensuring an accurate and fast temperature detection.

4 Compensating linear regulators

In *Figure 11* the high-level block diagram of linear regulators is shown.

The majority of cases of oscillations in LDO applications are caused by the ESR of the output capacitor being too high or too low. When selecting an output capacitor for an LDO, a solid tantalum capacitor is usually the best choice.

The value of the capacitor shouldn't be too small, otherwise it won't be able to prevent arising of high overshoots and undershoots on the output voltage.

LDO regulators require the ESR of the output capacitor to be within a certain range to assure regulator stability. Increasing the capacitor ESR will decrease the frequency of the zero in the transfer function consequently increasing the loop bandwidth but, when ESR is too high, there will not be enough phase margin at the unity gain frequency, eventually causing instability.

L5962 linear regulators have been designed to guarantee stability even when ceramic capacitors are applied to their output and thus ESR is very small, all over temperature range.

Consequently, it is just recommended to use capacitors with C > 0.5 µF for filtering the output of VSTBY, VLR1 and VLR2.

Figure 11. Linear regulator general block diagram

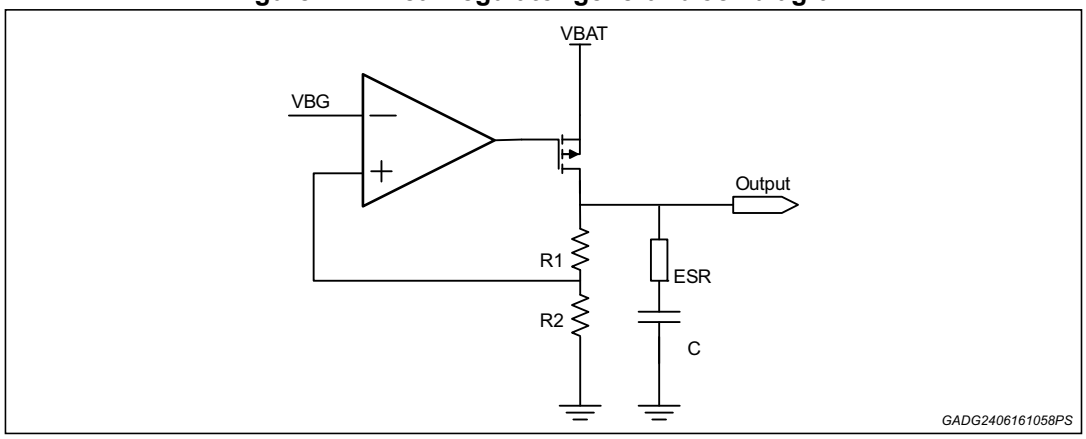
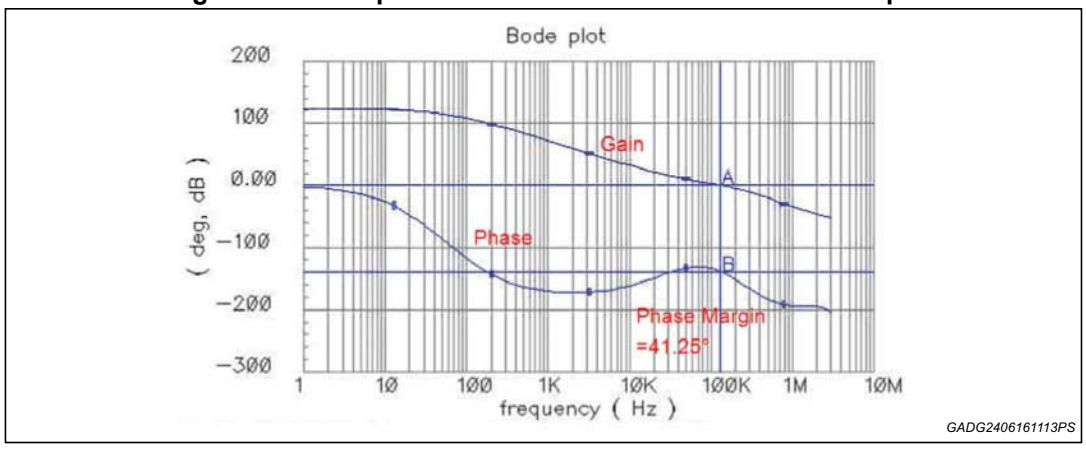


Figure 12. Bode plot of VLR1 with ESR = 0.1 Ω and C = 1 µF



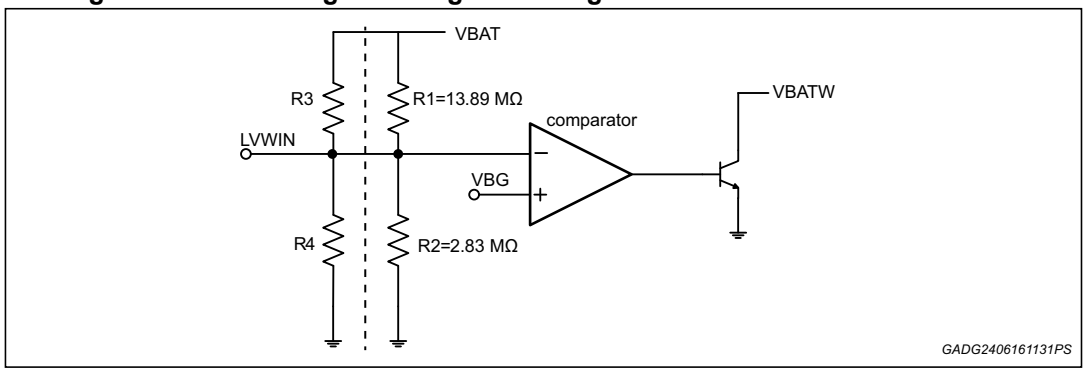
5 Trimming the threshold of low-voltage warning

Figure 13 shows the block diagram of L5962 Low-voltage Detector to which an external resistor divider R3-R4 has been connected.

By changing the values of R3 and R4 a trimming of the low-voltage detector threshold can be obtained: R3 and R4 values must be chosen in a way that, at the desired VBAT level to be detected, LVWIN pin voltage is equal to 1.25 V.

Being R1 and R2 in the range of MΩ, in order for the detection not to be affected by them R3 and R4 should be chosen with an order of magnitude of kΩ.

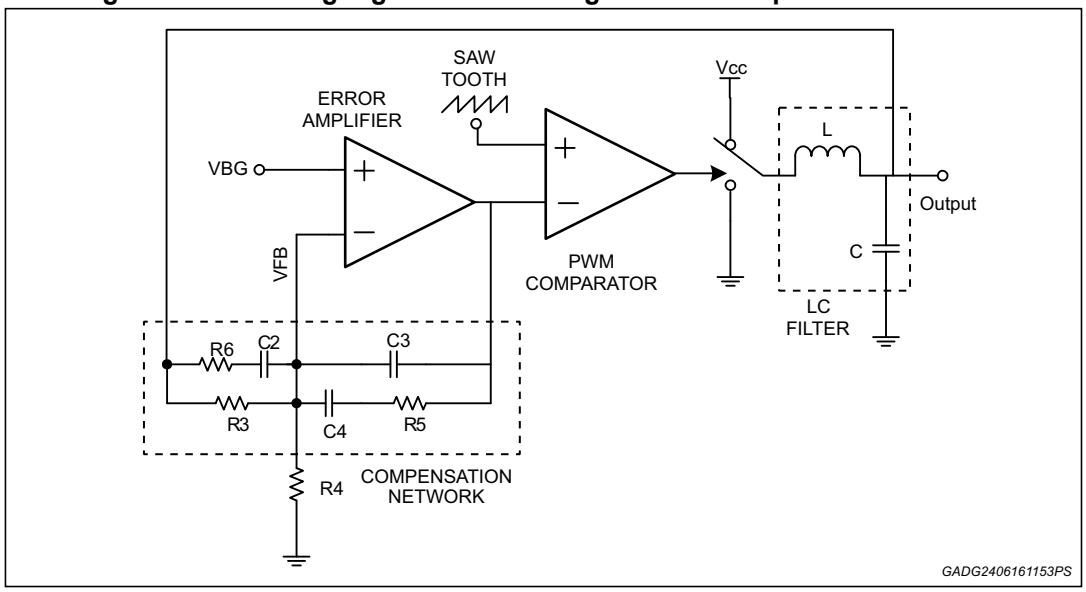
Figure 13. Low-voltage warning block diagram with external resistor divider



6 Compensating switching regulator

To compensate the switching regulator a Type-3 compensation network is suggested, realized by R6,C2,C3,R3,C4 and R5 as shown in *Figure 14*. This kind of network implements two zeroes to counteract the effects of the double pole introduced by output L-C filter, helping in stabilizing the system.

Figure 14. Switching regulator block diagram with compensation network



In the following paragraphs the transfer function of every block is described, to summarize all the singularities present in the regulation loop and thus allow the user to properly define external components values.

6.1 LC filter transfer function

The transfer function of LC filter is given by:

Equation 1

$$A_{LC}(s) = \frac{R_{LOAD}(1 + s \cdot ESR \cdot C)}{s^2 \cdot L \cdot C \cdot (ESR + R_{LOAD}) + s \cdot (ESR \cdot C \cdot R_{LOAD} + L) + R_{LOAD}}$$

where R_{LOAD} is defined as the ratio between V_{OUT} and I_{OUT}.

If R_{LOAD}>>ESR, the previous expression of A_{LC} can be simplified and becomes

Equation 2

$$A_{LC}(s) = \frac{1 + s \cdot ESR \cdot C}{s^2 LC + s \cdot ESR \cdot C + 1}$$

The zero of this transfer function is given by:

Equation 3

$$f_o = \frac{1}{2\pi \cdot ESR \cdot C}$$

f_o is the zero introduced by the ESR of the output capacitor and it is fundamental to increase the phase margin of the loop.

The poles of the transfer function can be calculated from the following expression:

Equation 4

$$f_{PLC1,2} = \frac{-ESR \cdot C \pm \sqrt{(ESR \cdot C)^2 - 4 \cdot L \cdot C}}{2 \cdot L \cdot C}$$

In the denominator of A_{LC} the typical second order system equation can be recognized:

Equation 5

$$s^2 + 2 \cdot \delta \cdot \omega_n \cdot s + \omega_n^2$$

If the damping factor δ is very close to zero, the roots of the equation become a double root whose value is ω_n.

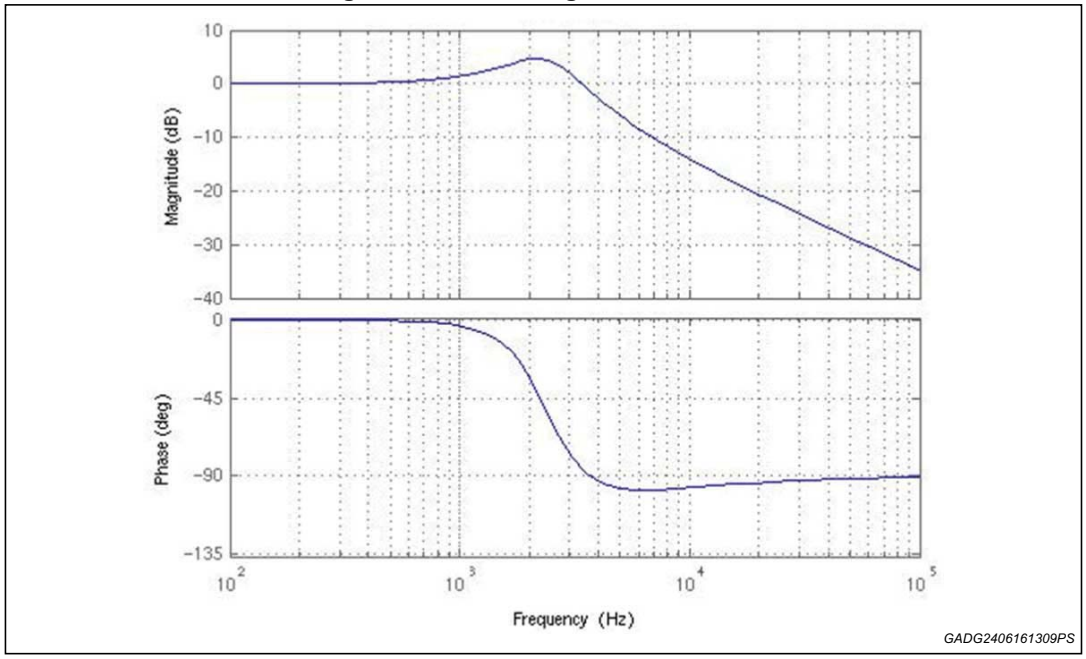
Similarly, for A_{LC} the poles can usually be defined as a double pole whose value is:

Equation 6

$$f_{PLC} = \frac{1}{2\pi\sqrt{L \cdot C}}$$

Given for instance L = 22 µH, C = 200 µF, ESR = 250 mΩ, the gain and phase bode diagram of LC filter are plotted in *Figure 15*.

Figure 15. Bode diagram of LC filter



6.2 PWM comparator transfer function

The PWM comparator compares the sawtooth signal and the Error Amplifier output signal.

Its transfer function is given by the following formula:

Equation 7

$$G_{PWM}(s) = \frac{V_{CC}}{\Delta V_{OSC}}$$

where ΔV_{OSC} is the peak to peak voltage of the oscillator: when the switching frequency is determined by the internal oscillator ΔV_{OSC} = 2.3 V, while if the switching frequency is forced with a SYNC signal to f=400kHz, ΔV_{OSC} = 1.2188 V.

Being the relationship between fsw and ΔV_{OSC} linear, ΔV_{OSC} for other switching frequencies can be deduced starting from these two values.

Considering V_{CC} = 14 V, G_{PWM} value is 6.08695 in free-run condition and 11.4867 at 400 kHz respectively.

6.3 Error amplifier and compensation network

The transfer function (equation1) for the output filter shows the well known double pole of an LC filter. It is very important to note that the ESR of capacitor is very small, so the system phase will experience a very sharp decrement at the double pole frequency while the gain will have a rather high peak. Systems that have such output filter are more difficult to compensate since the phase will need an extra boost to provide the necessary phase margin for stability. In these cases a Type-3 compensation is typically used to achieve stability.

Figure 16 shows the block diagram of Error Amplifier and the Type-3 compensation network, consisting of R6, C2, R3, C3, C4 and R5, that introduce two poles, two zeros and a pole at 0Hz frequency.

The transfer function of the error amplifier and its compensation network is:

Equation 8

$$A_0(s) = \frac{(1 + s \cdot R5 \cdot C4)[1 + s \cdot (R3 + R6) \cdot C2]}{s \cdot R3 \cdot (C3 + C4)(1 + s \cdot R6 \cdot C2)\left[\frac{1 + s \cdot R5 \cdot C3 \cdot C4}{(C3 + C4)}\right]}$$

The poles of this transfer function are:

Equation 9

$$f_{P0} = \frac{1}{2\pi \cdot R3 \cdot (C3 + C4)}$$

Equation 10

$$f_{P1} = \frac{1}{2\pi \cdot R6 \cdot C2}$$

Equation 11

$$f_{P2} = \frac{1}{2\pi \cdot R5 \cdot \frac{C3 \cdot C4}{(C3 + C4)}}$$

While the zeroes are defined as:

Equation 12

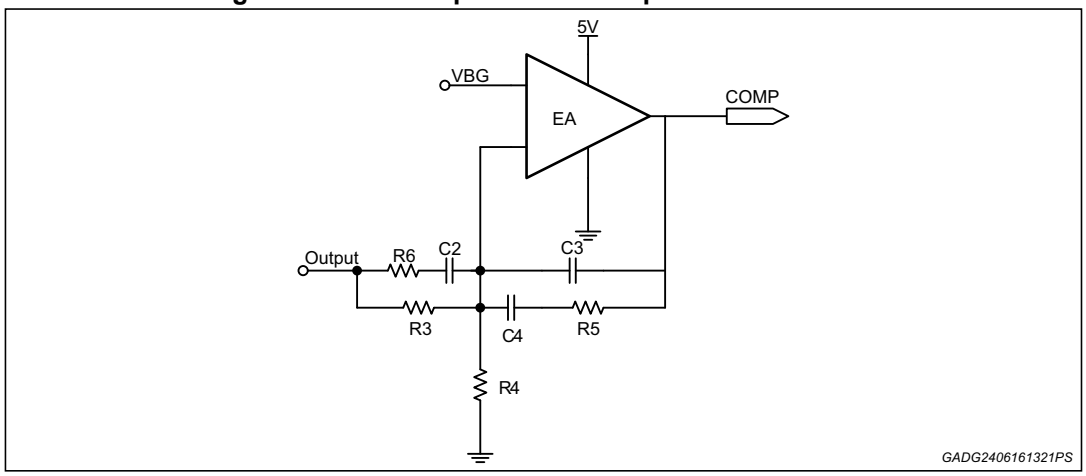
$$f_{z1} = \frac{1}{2\pi \cdot R5 \cdot C4}$$

Equation 13

$$f_{z2} = \frac{1}{2\pi \cdot (R3 + R6) \cdot C2}$$

f_{z1} and f_{z2} are usually set near the LC filter double pole frequency to increase the phase margin while f_{p1} and f_{p2} are usually set at high frequency in order to reduce the high frequency gain.

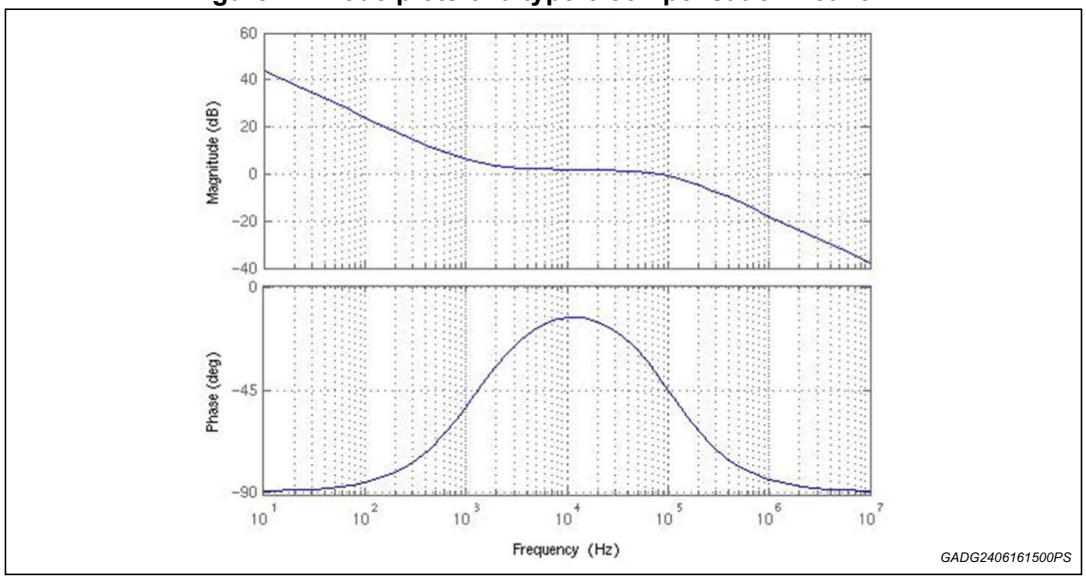
Figure 16. Error amplifier and compensation network



Following these indications and considering for example L = 22 µH, C = 200 µF the following set of values is determined: R6 = 470 Ω, R3 = 22 kΩ, C2 = 3.3 nF, C3 = 2.7 nF, C4 = 1.8 nF, R5 = 75 kΩ.

Bode plots of this type-3 compensation network are plotted in *Figure 17*.

Figure 17. Bode plots of a type-3 compensation network



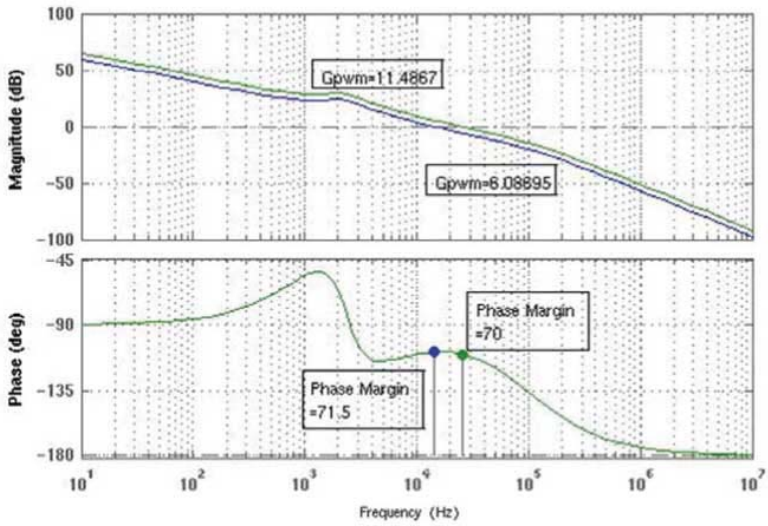
6.4 Examples of system compensation: impact of ESR

Case 1

- C = 2 x 100 µF electrolytic capacitors (total ESR = 0.25 Ω) with a 2.2 µF ceramic capacitor in parallel; L = 22 µH
- R6 = 470 Ω, R3 = 22 kΩ, R4 = 22 kΩ/(VDCOUT-1), (VDCOUT = 1.2~8V), C2 = 3.3 nF, C3 = 2.7 nF, C4 = 1.8 nF, R5 = 75 kΩ
- G_{PWM} = 6.08695 (free-run) or 11.4867 (400 kHz)

Open-loop gain/phase Bode plots are plotted in *Figure 18*.

Figure 18. Case 1 open-loop Bode plots



The unit gain bandwidth and phase margin are:

f_{C1} = 14.3 kHz Phase margin = 71.5° (free-run)

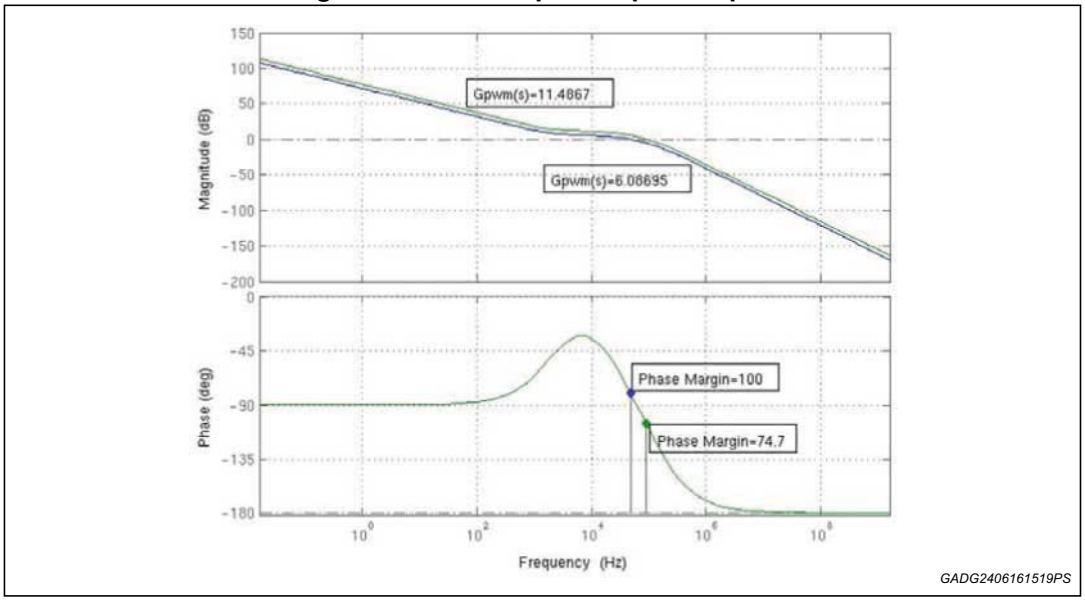
f_{C2} = 25.6 kHz Phase margin = 70° (400kHz)

Case 2

- C = 220 µF electrolytic capacitor (ESR = 4 Ω) + 1 x 2.2 µF ceramic capacitor; L = 22 µH
- R6 = 330 Ω, R3 = 22 kΩ, R4 = 3.1 kΩ (VDCOUT = 8), C2 = 3.3 nF, C3 =10 nF, C4 = 1 nF, R5 = 75 kΩ
- GPWM = 6.08695 or 11.4867

Open-loop gain/phase Bode plots are plotted in *Figure 19*.

Figure 19. Case 2 open-loop Bode plots



Under the conditions above, the unit gain bandwidth and phase margin are:

f_{C1} = 48.2 kHz Phase margin = 100° (free_run)

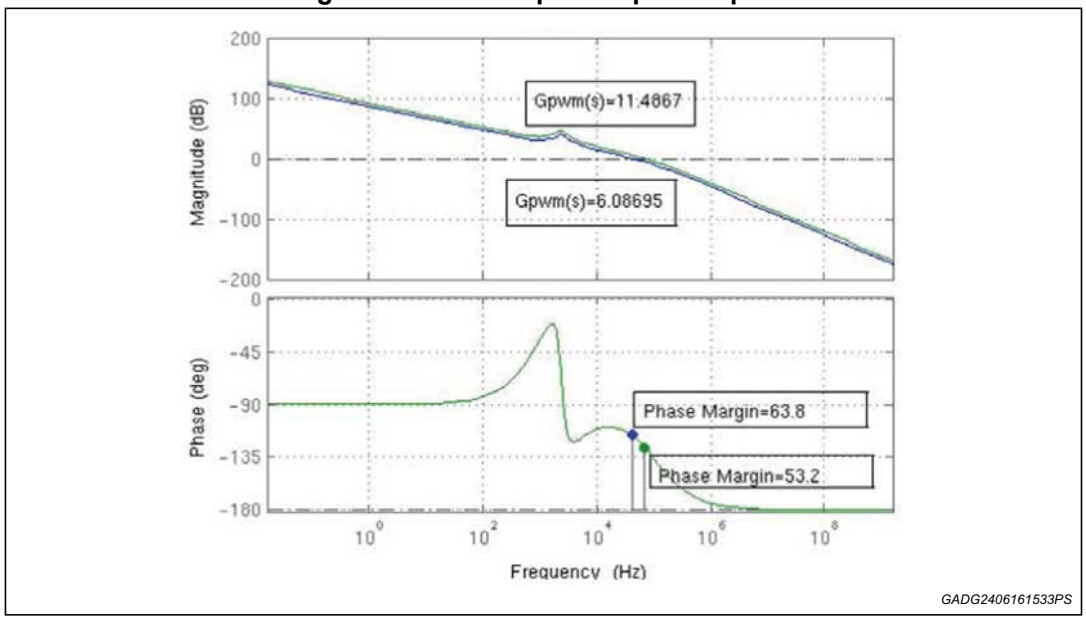
f_{C2} = 90.3 kHz Phase margin = 74.7° (400 kHz)

Case 3

- C = 2 x100 µF tantalum capacitor (ESR = 0.1 Ω) + 1 x 2.2 µF ceramic capacitor; L = 22 µH
- R6 = 470 ΩW, R3 = 22 kΩ, R4 = 22 kΩ (VDCOUT-1), (VDCOUT = 1.2~8 V), C2 = 3.3 nF, C3 = 330 µF, C4 = 1.8 nF, R5 = 75 kΩ
- GPWM = 6.08695 or 11.4867

Open-loop gain/phase Bode plots are plotted in *Figure 20*.

Figure 20. Case 3 open-loop Bode plots



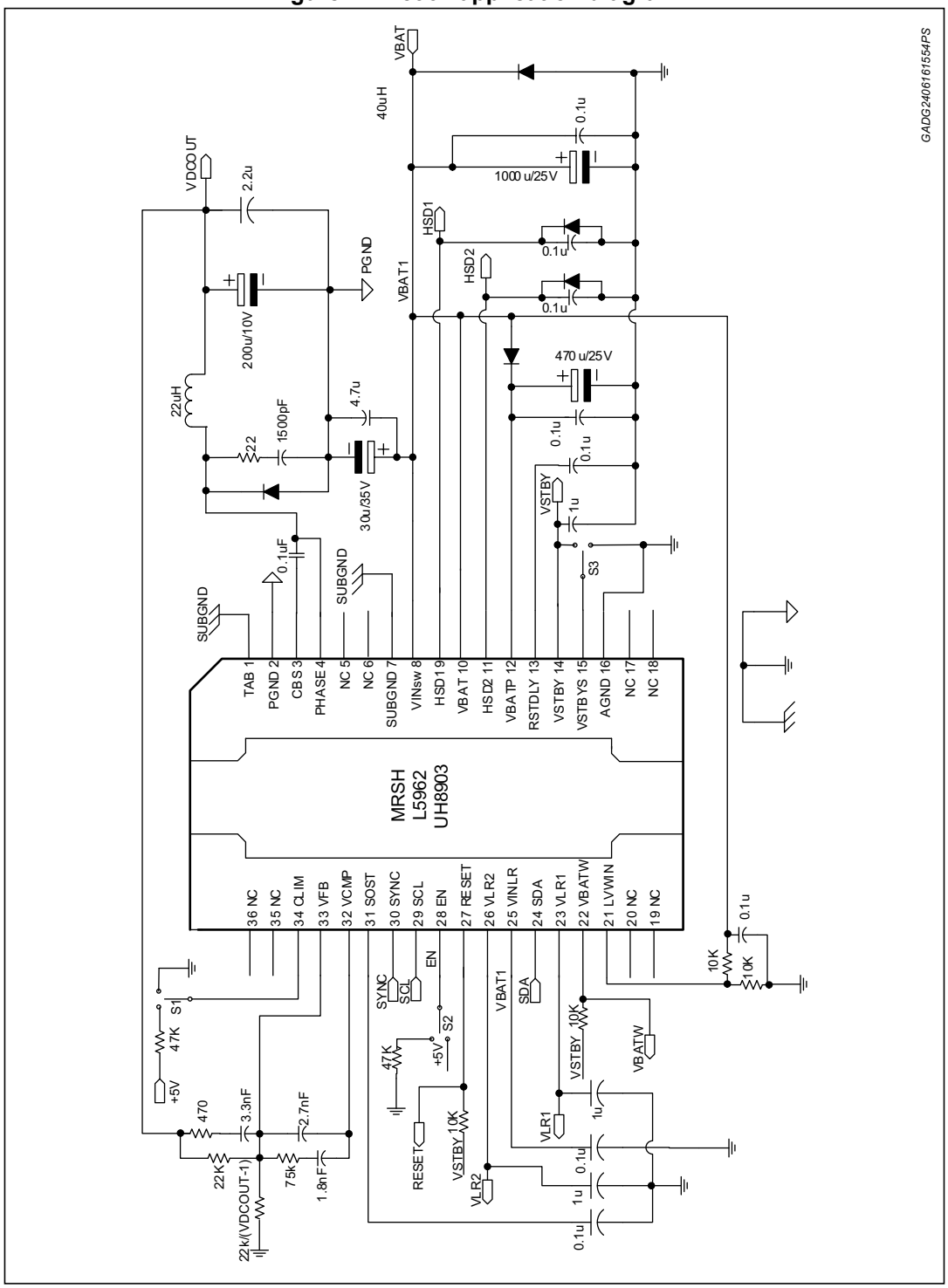
Under the conditions above, the unit gain bandwidth and phase margin are:

f_{C1}= 41.9 kHz Phase margin = 63.8° (free-run)

f_{C2} =70.2 kHz Phase margin = 53.2° (400 kHz)

7 Application diagram

Figure 21. L5962 application diagram



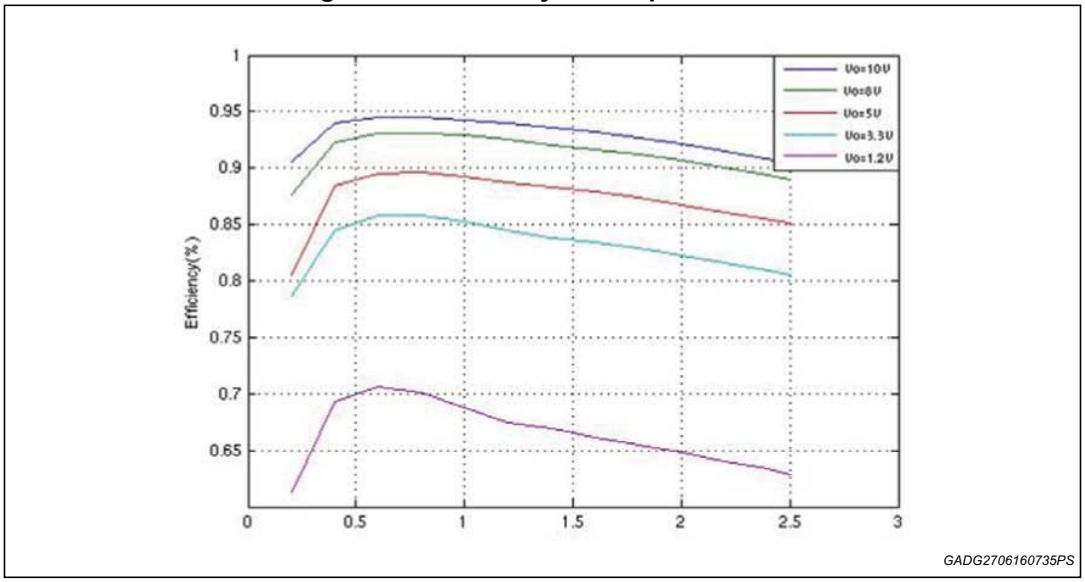
Note: As stated in Figure 21: L5962 application diagram, the correct device behavior is guaranteed with pin 8, 10 and 12 connected to a unique supply source VBAT.

8 Device performance

Performance mentioned in the following paragraphs have been tested in these conditions: Vcc = 14.4V, T = 25°C, switching regulator in free-run condition.

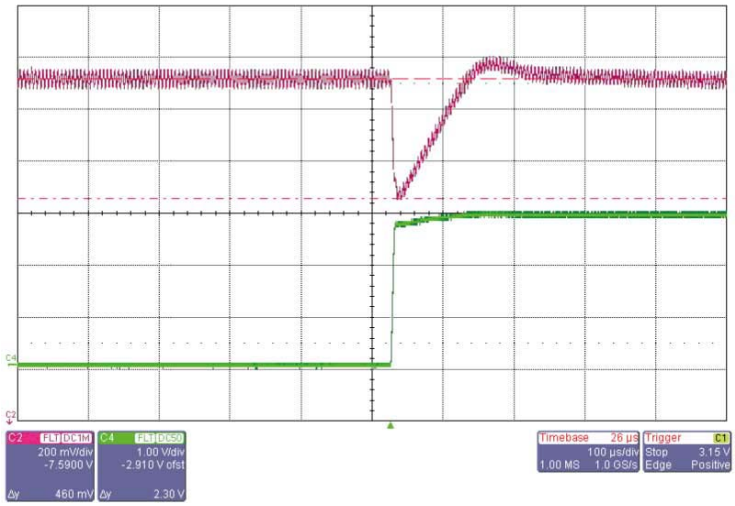
8.1 Switching regulator efficiency

Figure 22. Efficiency vs. output current



8.2 Switching regulator transient response

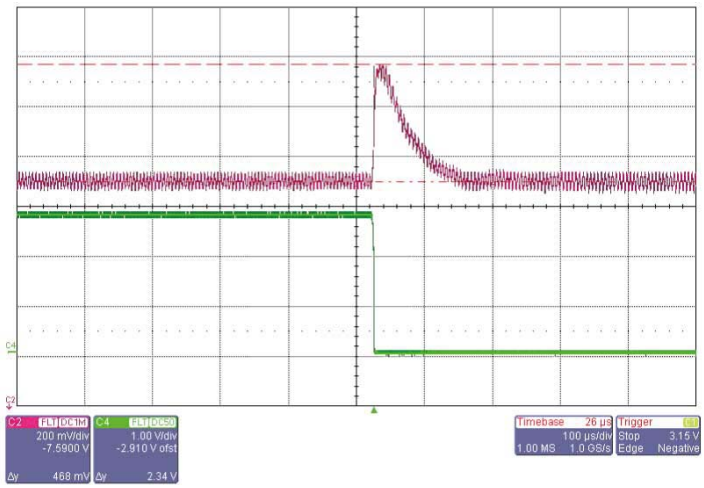
Figure 23. Switching regulator undershoot



V_{out} = 8.09 V (C2), I_{LOAD} (C4) varying from 0 to 2.87 A => undershoot = 460 mV

GADG2706160743PS

Figure 24. Switching regulator overshoot

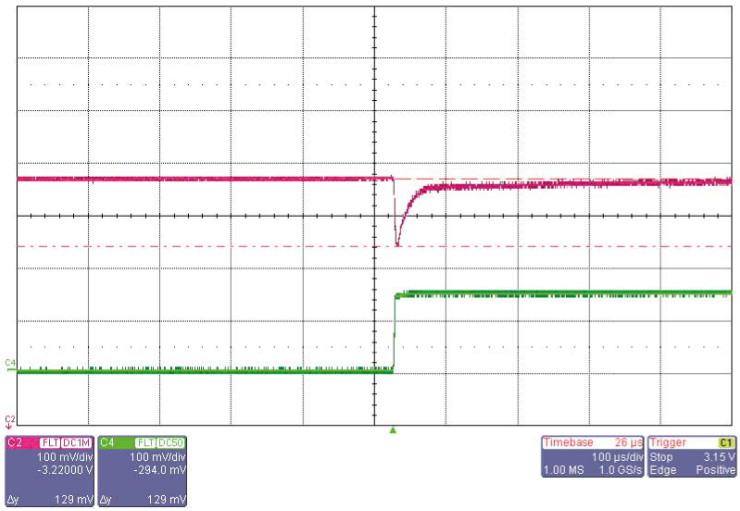


V_{out} = 8.09 V (C2), I_{LOAD} (C4) varying from 2.75 A to 0 A => undershoot = 468 mV

GADG2706160844PS

8.3 VSTBY transient response

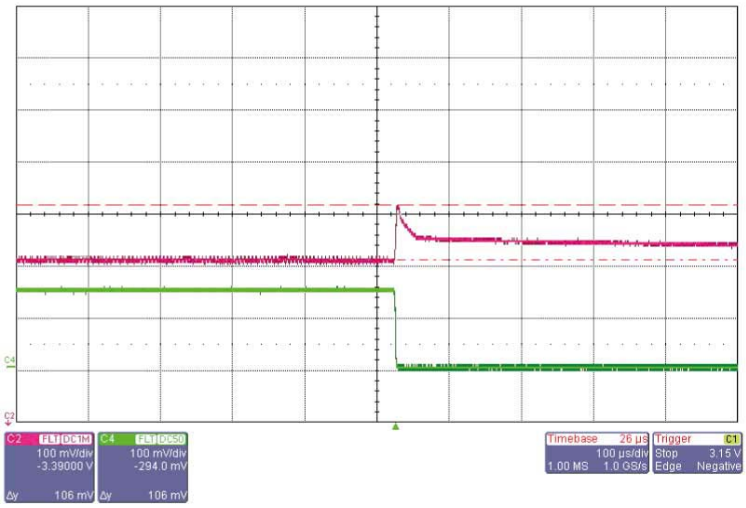
Figure 25. VSTBY undershoot



VSTBY = 3.31 V (C2), I_{LOAD} (C4) varying from 0 to 150 mA => undershoot = 129 mV

GADG2706160856PS

Figure 26. VSTBY overshoot

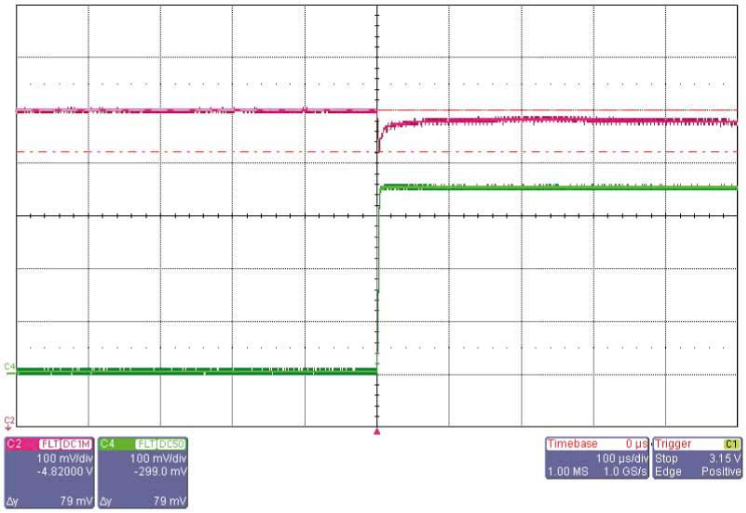


VSTBY = 3.31 V (C2), I_{LOAD} (C4) varying from 150 mA to 0 => undershoot = 106 mV

GADG2706160905PS

8.4 VLR1 transient response

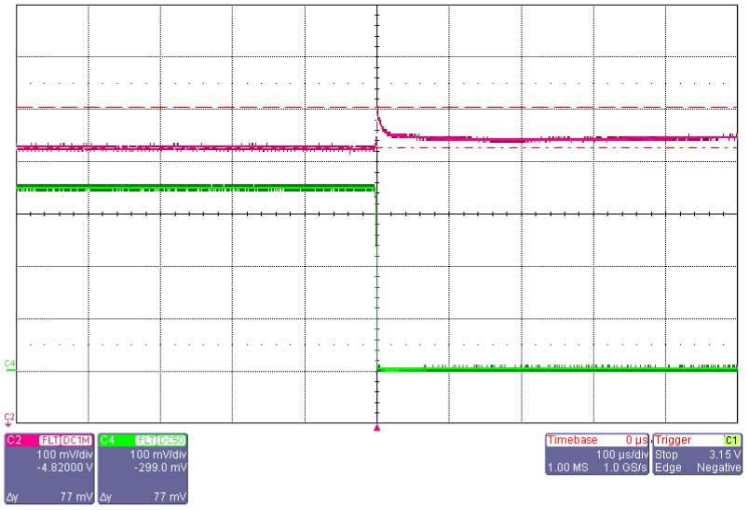
Figure 27. VLR1 undershoot



VLR1 = 5.05 V (C2), I_{LOAD} (C4) varying from 0 to 357.8 mA => undershoot = 68 mV

GADG2706160929PS

Figure 28. VLR1 overshoot

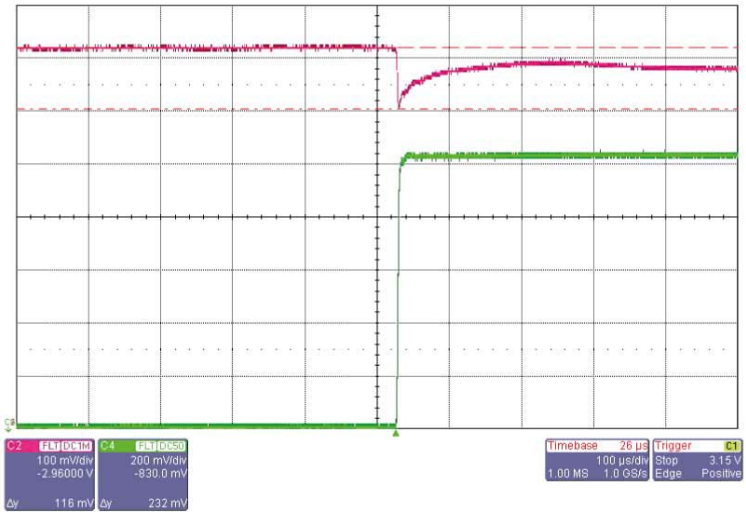


VLR1 = 5.05 V (C2), I_{LOAD} (C4) varying from 355.7 mA to 0 A => overshoot = 80 mV

GADG2706160934PS

8.5 VLR2 transient response

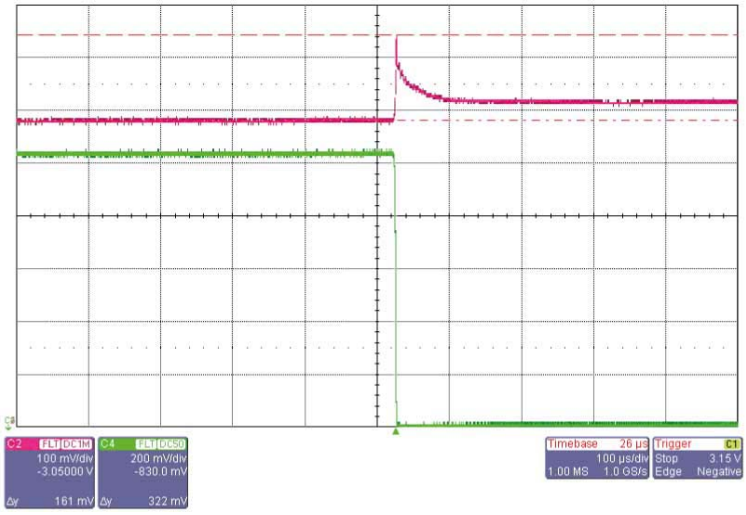
Figure 29. VLR2 undershoot



VLR2 = 3.3 V (C2), I_{LOAD} (C4) varying from 0 to 1.07 A => undershoot = 102 mV

GADG2706160940PS

Figure 30. VLR2 overshoot



VLR2 = 3.3 V (C2), I_{LOAD} (C4) varying from 1.07 A to 0 A => undershoot = 124 mV

GADG2706160945PS

9 Device utilization hints

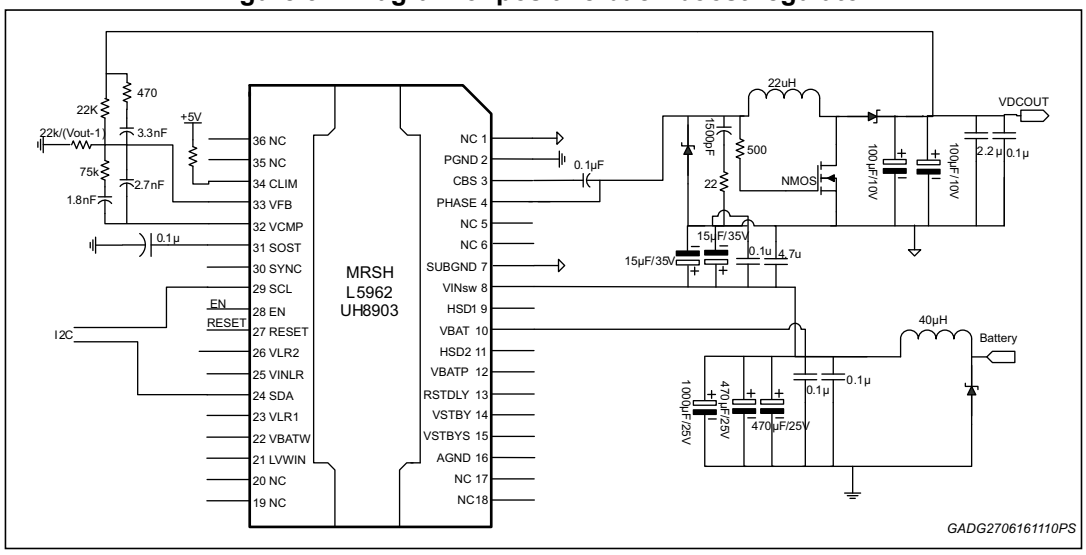
9.1 Positive-output buck-boost regulator

L5962 can be used to realize an Up-Down converter with a positive output voltage. In *Figure 31* is shown the schematic circuit of this topology.

The output voltage is given by $V_O = V_{IN} \cdot D/(1-D)$, where D is the duty cycle. The output current is equal to $I_{OUT} = I \cdot (1-D)$.

When $I_{LOAD} = 0$, the input voltage VBAT can range from 3.55 V to 28.5 V.

Figure 31. Diagram of positive buck-boost regulator



At a fixed output level the current capability of this topology is limited by the DC/DC converter OCP circuits: setting VDCOUT = 10/8/5/3.3/1.2V, *Figure 32*/*33*/*34*/*35*/*36*/ show the relationship between maximum load current (Maximo) and battery voltage (VBAT).

Figure 32. Maximum output current vs. input voltage VBAT in buck-boost config. (VDCOUT = 10 V)

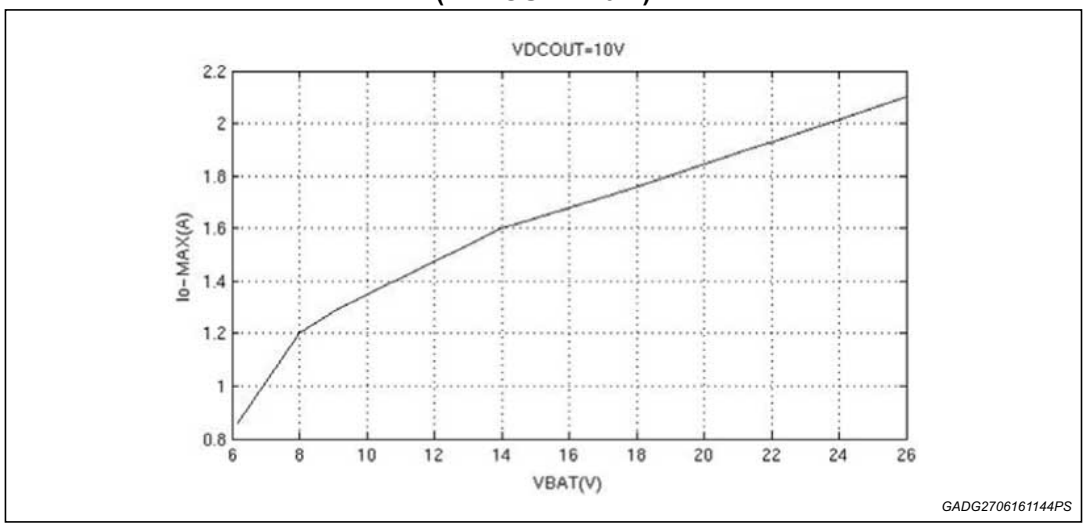


Figure 33. Maximum output current vs. input voltage VBAT in buck-boost config. (VDCOUT = 8 V)

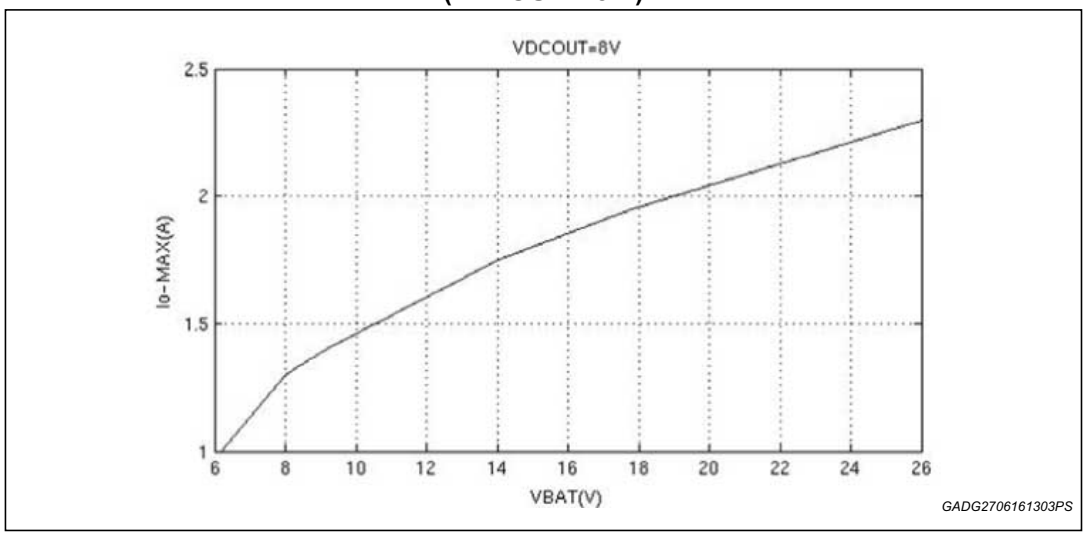


Figure 34. Maximum output current vs. input voltage VBAT in buck-boost config. (VDCOUT = 5 V)

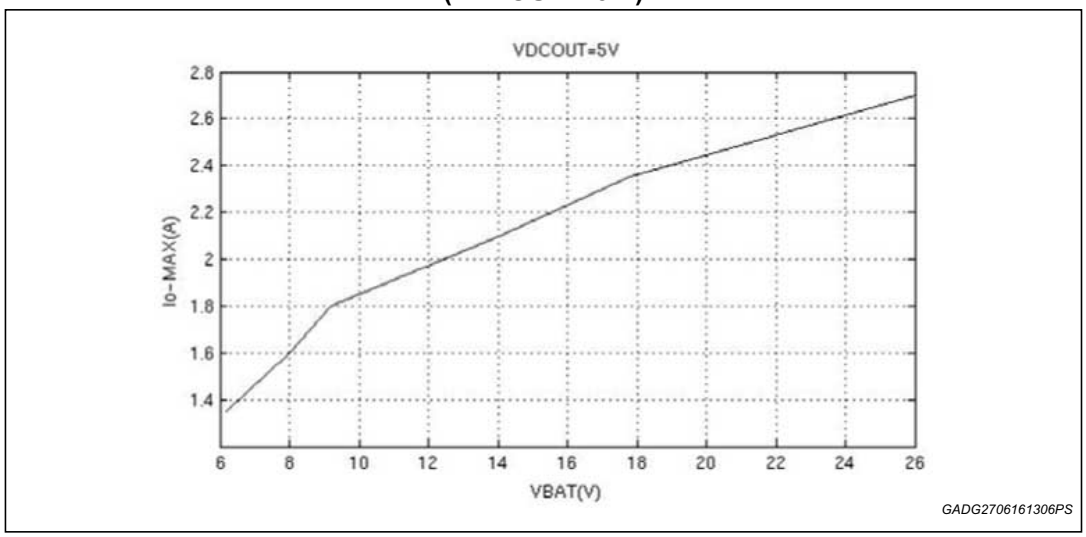


Figure 35. Maximum output current vs. input voltage VBAT in buck-boost config. (VDCOUT = 3.3 V)

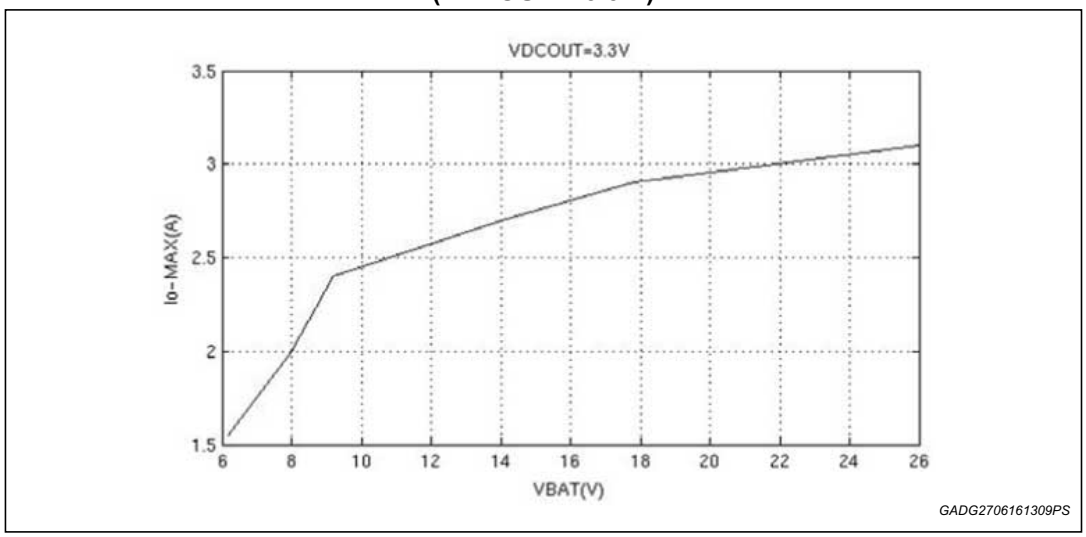


Figure 36. Maximum output current vs. input voltage VBAT in buck-boost config. (VDCOUT = 1.2 V)

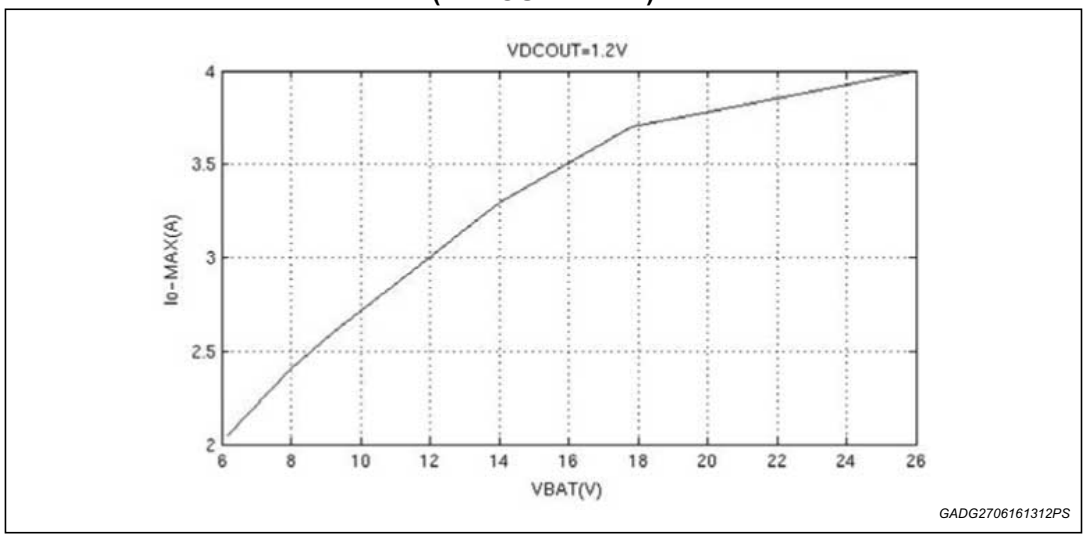
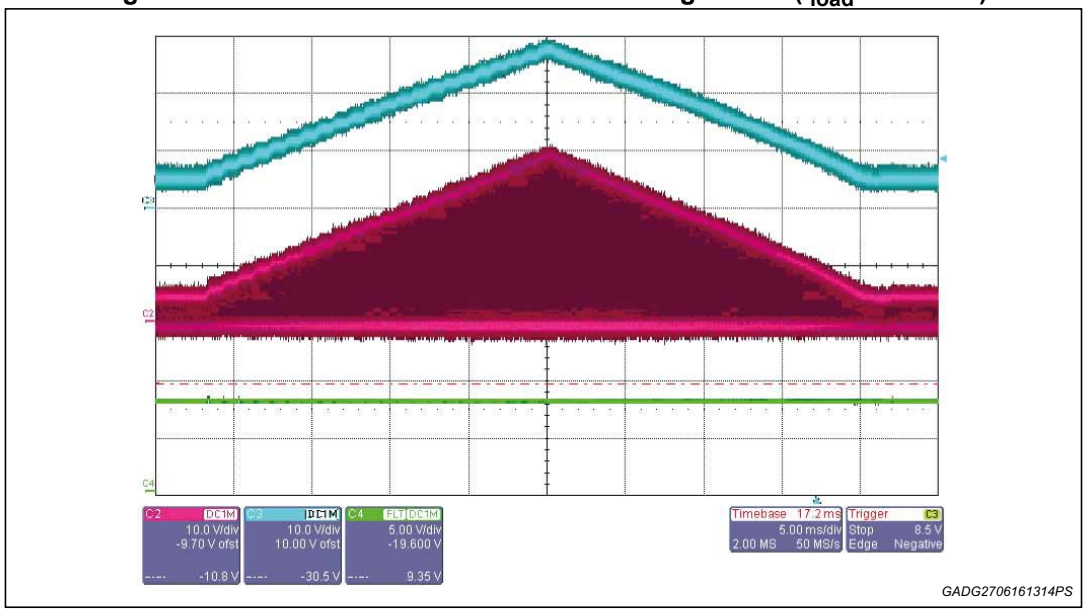


Figure 37 shows buck-boost behavior in the case Iload=500mA (C3 = VBAT, C2 = PH, C4 = V_{out}).

VBAT varies from 5.25V to 28.3V and then from 28.3V to 5.25V: PH amplitude varies accordingly, while Vout is kept perfectly constant by the regulator.

Figure 37. L5962 behavior in buck-boost configuration (I_{load} = 500 mA)



10 Revision history

Table 2. Document revision history

Date	Revision	Changes
08-Sep-2008	1	Initial release.
18-Sep-2013	2	Updated Disclaimer.
27-Jun-2016	3	Added Note: *As stated in Figure 21: L5962 application diagram, the correct device behavior is guaranteed with pin 8, 10 and 12 connected to a unique supply source VBAT. on page 24*