
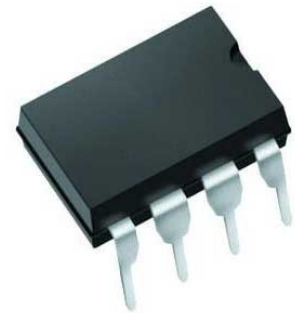


## FPGA Configuration PROM Memories

<b>Manufacturer:</b>	<a href="#">AMD Xilinx, Inc</a>
<b>Package/Case:</b>	DIP8
<b>Product Type:</b>	Programmable Logic ICs
<b>RoHS:</b>	RoHS Compliant/Lead free 
<b>Lifecycle:</b>	Obsolete



Images are for reference only

[Inquiry](#)

## General Description

The Spartan family of PROMs provides an easy-to-use, cost-effective method for storing Spartan device configuration bitstreams.

When the Spartan device is in Master Serial mode, it generates a configuration clock that drives the Spartan FPGA PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the Spartan device DIN pin. The Spartan device generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When a Spartan device is in Slave Serial mode, the PROM and the Spartan device must both be clocked by an incoming signal.

For device programming, either the Xilinx Alliance or the Foundation series development systems compiles the Spartan device design file into a standard HEX format which is then transferred to most commercial PROM programmers.

## Recommended For You

### [XCF128XFT64C](#)

AMD Xilinx, Inc

BGA

### [XC18V04VQ44I](#)

AMD Xilinx, Inc

QFP

### [XC17128EPD8I](#)

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DIP8

### [XC1765ELSO8C](#)

AMD Xilinx, Inc

SOP8

### [XC18V04VQ44C](#)

AMD Xilinx, Inc

QFP44

### [XC18V01SO20C](#)

AMD Xilinx, Inc

SOP20

### [XC18V04VQG44C](#)

AMD Xilinx, Inc

QFP

### [XCF32PVOG48C](#)

AMD Xilinx, Inc

TSOP48

### [XC18V01PCG20C](#)

AMD Xilinx, Inc

PLCC20

**XCF04SVO20C**

AMD Xilinx, Inc

TSSOP20

**XC2C256-7CPG132I**

AMD Xilinx, Inc

BGA132

**XCF04SVOG20C**

AMD Xilinx, Inc

TSSOP20

**XCF08PFS48C**

AMD Xilinx, Inc

BGA

**XC18V01VQ44C**

AMD Xilinx, Inc

TQFP44

**XC1765EPD8C**

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